

INTEGRATED CIRCUITS

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MC511, MC561/MC411, MC461

MC510, MC560/MC410, MC460

MC509, MC559/MC409, MC459

LINE DRIVERS MC507, MC557/MC407, MC457

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EXPANDERS		
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Dual 4-Input Expander for NAND Gates

4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates

Dual 4-Input Expander for AND-OR-INVERT Gates

Dual 4-Input Line Driver

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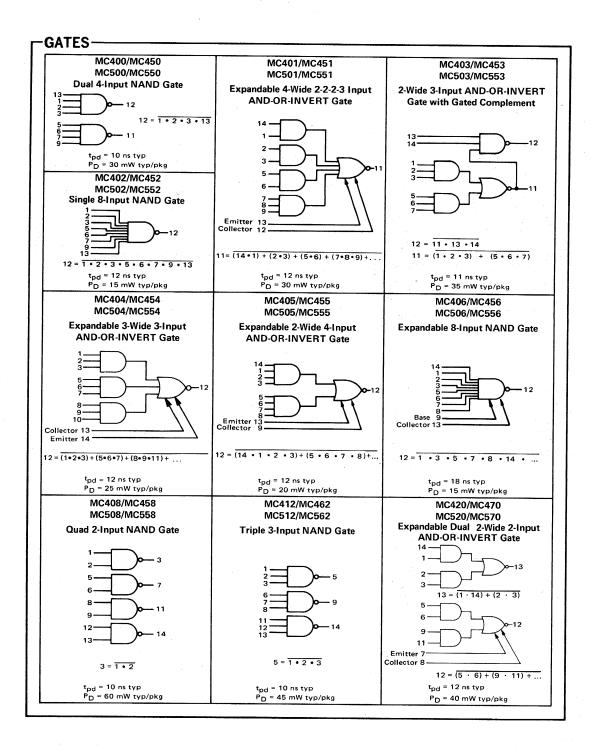
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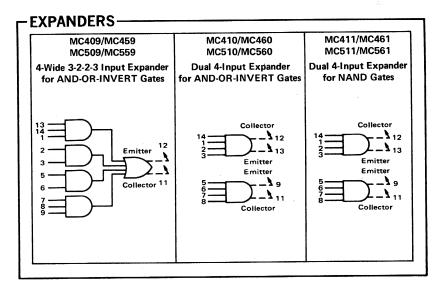
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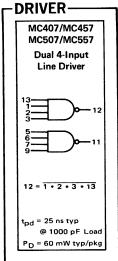
NUMERICAL INDEX (Functions and Characteristics)

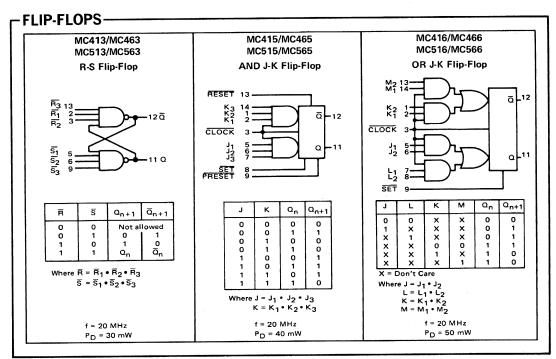
 $V_{CC} = 5.0 \text{ V, } T_A = 25^{\circ}\text{C}$

*1 -		ype	Loa Fa	tput ding ctor Output	Propagation	Power		
Function	Case 609, 93 0 to +75°C	Case 609 -55 to +125 ^o C	MC400 Series	MC500 Series	Delay ^t pd ns typ	Dissipation mW typ/pkg	Page No.	
Dual 4-Input NAND Gate	MC400 MC450	MC500 MC550	12 ⁻	15 7	10	30	4-14	
Expandable 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate	MC401 MC451	MC501 MC551	12 6	15 7	12	30	4-24	
Single 8-Input NAND Gate	MC402 MC452	MC502 MC552	12 6	- 15 7	12	15	4-10	
2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement	MC403 MC453	MC503 MC553	12 6	15 7	11	35	4-27	
Expandable 3-Wide 3-Input AND-OR-INVERT Gate	MC404 MC454	MC504 MC554	12 6	15 7.	12	25	4-20	
Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC405 MC455	MC505 MC555	12 6	15 7	12	20	4-10	
Expandable 8-Input NAND Gate	MC406 MC456	MC506 MC556	12 6	15 7	18	15	4-1	
Line Driver	MC407 MC457	MC507 MC557	12 6	15 7	25 @ 1000 pF Load	60	4-50	
Quad 2-Input NAND Gate	MC408 MC458	MC508 MC558	12	15 7	10	60	4-2	
4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates	MC409 MC459	MC509 MC559	12 6	15 7	_	_	4-4	
Dual 4-Input Expander for AND-OR-INVERT Gates	MC410 MC460	MC510 MC560	12 6	15 7	_		4-4	
Dual 4-Input Expander for NAND Gates	MC411 MC461	MC511 MC561	12 6	15 7	_	-	4-4	
Triple 3-Input NAND Gate	MC412 MC462	MC512 MC562	12 6	15 7	10	45	,4-1	
R-S Flip-Flop	MC413 MC463	MC513 MC563	12 6	15 7	f = 20 MHz	30	4-4	
AND J-K Flip-Flop	MC415 MC465	MC515 MC565	12 6	15 7	f = 20 MHz	40	4-3	
OR J-K Flip-Flop	MC416 MC466	MC516 MC566	12 6	15 7	f = 20 MHz	50	4-3	
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC420 MC470	MC520 MC570	12 6	15 7	12	40	4-3	











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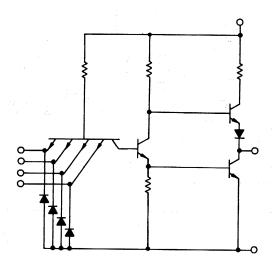
INTRODUCTION

MTTL transistor-transistor logic is a medium speed, high-noise-immunity family of saturating integrated logic circuits.

The circuits in the MTTL family are identified by a multiple emitter input transistor and an active "pull-up" in the upper output network as shown in Figure 1.

The multiple emitter input configuration offers the maximum amount of logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The active pull-up output configuration provides low impedance in the high output state. The resulting low impedances in both states provide excellent ac noise immunity and allow high-speed operation while driving large capacitive loads.

FIGURE 1 - TYPICAL MTTL CIRCUIT



MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage — Continuous MC500 Series MC400 Series	+8.0 +7.0	Vdc
Supply Operating Voltage Range	4.5 to 6.0	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range MC500 Series MC400 Series	-55 to +125 0 to +75	°c
Storage Temperature Range Flat Package Plastic Package	-65 to +200 -55 to +125	°c
Maximum Junction Temperature MC500/550 Series MC400/450 Series	+175 +150	°c
Thermal Resistance - Junction To Case $(\theta_{ m JC})$ Ceramic Flat Package Plastic Dual-In-Line	0.09 0.15	°C/m\
Thermal Resistance - Junction To Ambient (θ _{JA}) Ceramic Flat Package Plastic Dual-In-Line	0.26 0.30	°C/m\

MTTL

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TYPICAL CHARACTERISTICS

The following summary presents the typical operating characteristics of the MTTL family. Unless otherwise indicated, the parameters are defined for VCC = +5.0 volts and T_A = +25°C.

Supply Voltage Operating Range = 4,5 to 6.0 volts

Operating Temperature Range: MC500/550 Series = -55 to +125°C MC400/450 Series = 0 to +75°C

Output Drive Capability

Other Gates (Output Loading Factor):

MC500 Series = 15 MC500 or MC550 Series Gates.

MC550 Series = 7 MC500 or MC550 Series Gates.

MC400 Series = 12 MC400 or MC450 Series Gates. MC450 Series = 6 MC400 or MC450 Series Gates.

Capacitance = 600 pF

Output Impedance

High State = 70 ohms (unsaturated) nominal

Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits +5.5 volts maximum -0.5 volt minimum Switching Threshold = 1.5 volts nominal

Input Impedance

High State = 400 k ohms nominal Low State = 4.0 k ohms nominal

Worst-Case DC Noise Margin

High State - MC500/550 series 0.700 volt minimum MC400/450 series 0.600 volt minimum

Mindred & Commission

Low State - MC500/550 series 0,750 volt minimum MC400/450 series 0,750 volt minimum

Power Dissipation 15 mW per gate typical

40-50 mW per flip-flop typical

Switching Speeds 1 Average Propagation Delay = 10 ns per gate typical 18 ns per flip-flop typical

Rise Time = 2.5 ns typical Fall Time = 1.5 ns typical

Flip-Flop Clock Frequency (MC515/516 Series) = 20 MHz maximum.

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL, the designer must continually be aware of the fact that he is working with the fastest form of saturating logic available in the industry today. The switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions have been included to help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rate of change of currents and voltages for a single MTTL gate is in the range of 10⁷ A/s and 10⁸ V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL circuits. A comparatively large, low-inductance type capacitor (in the 1.0 μ F range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 μ F capacitors for every eight packages throughout a breadboard is adequate to supress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving alarge capacitive load.

Power Dissipation

The standard supply voltage of the MTTL logic circuits is +5.0 Vdc.The typical average dc power dissipation is given for each MTTL circuit. (2) It should be noted that the totem pole output common to all high level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.35 mW/MHz/output for a 15 pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL circuits.

Unused Inputs and Unused Gates

The unused inputs of any. MTTL logic circuit should not be left open, and can either be tied to the used inputs or returned to the supply voltage. This will reduce any potential problems resulting from external noise. If the inputs are returned to the supply voltage, care should be taken to insure that the supply voltage does not exceed the maximum rated input voltage of 5.5 volts. If the supply can exceed 5.5 volts, the unused inputs must be returned to a lower voltage. The total number of inputs that can be tied to the output of any driving gate is 50. (This is defined as high state output loading rules must still be maintained. The minimum logical "1" level for the high state output loading is summarized for VCC = 5.0 V, VIL = 0.45 V and IOH = -5.0 mA:

MC500/550 Series - V_{OH} = 2.8 volts minimum @ -55° C MC400/450 Series - V_{OH} = 3.0 volts minimum @ 0° C

The unused inputs of the various flip-flops may be tied back to their associated outputs. To determine which outputs are related to each set of inputs by internal feedback, refer to the circuit schematics.

The inputs of any unused gate in a package should be grounded. This places the gate in its lowest power condition and will help to eliminate unnecessary power drain.

Expanders and Expander Nodes

The ORing nodes of all the MTTL AND-OR-INVERT gates are made available for expanding the number of AND gates to 10. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capácitance added to the expander nodes is typically 1.0 ns/pF.

Output OR (AND) Function

Unlike the MDTL family of logic circuits, the outputs of the MTTL logic circuits cannot be tied together to perform the output OR, or more correctly, the output AND function. If the outputs of the MTTL family devices are tied together, it would be possible for the lower output transistor of one circuit and the upper output transistor of another circuit to be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground and the current that flows (approximately I_{SC}) exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

Operating Characteristics of Flip-Flops

The general operating characteristics and restrictions for the MC515/MC516 series J-K flip-flops are as follows:

The clocked inputs are inhibited when the clock is in the low state, and data should be applied and allowed to settle. The clocked inputs are enabled when the clock goes high and data enters the flip-flop. The data is temporarily stored in the charge-storage section (temporary memory) while the clock is in the high state. This data is transferred to the bistable section on the negative clock transition.

The data on the clocked inputs should not be changed while the clock is in the high state. Data changes during this clock condition require 300 ns settling time.

require 300 ns settling time.

The direct SET, PRESET, and RESET inputs do not directly affect the charge-storage section and therefore should not be used while the clock is high. On the negative transition of the clock, previously stored data may override the asynchronous set output state. Further, the direct SET, PRESET, and RESET inputs do not

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override the clock and will not control the state of the flip-flop until 120 ns after the negative transition of the clock. The clock signal must conform to the following boundary conditions at +125°C.

Maximum guaranteed clock frequency	= 20 MHz
Maximum clock fall time	= 150 ns
Minimum clock pulse width	= 20 ns
Minimum clock pulse amplitude	= 1.8 V
Maximum negative clock voltage	= -0 5 V

Note: These boundary conditions for operation are not defined as occuring simultaneously.

The transfer of data from the charge storage section to the bistable section is essentially an ac operation and thus results in the testriction of the clock fall time. If the clock fall time is greater than 150 ns, the information retained in the charge-storage section may not be transferred to the bistable section. The flip-flop will operate from very low frequencies to 20 MHz as long as the clock fall time is less than or equal to 150 ns.

Large negative clock excursions may cause incorrect data transfers to the bistable section during the transfer cycles. Therefore, the most negative clock signal should be limited to -0.5 volt.

(1) The switching characteristics of the MTTL family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turnon delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2}$$
 ns.

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative transition of the output from the 2.0 V to the 1.0 V level.

$$P_{D} = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where IpDL and IpDH are the typical dc current drains at VCC = +5.0 V.

MC400/450 and MC500/550 MTTL* series integrated circuits are electrically interchangeable with SUHL I[†] series logic circuits.

SG SF		-55 to	+125°C	0 to +	75°C
NUMBERS	Description	Fan-Out = 15	Fan-Out = 7	Fan-Out = 12	Fan-Out = 6
SG40-43	Dual 4-Input NAND Gate	MC500	MC550 .	MC400	MC450
SG50-53	Expandable 2-Wide 2-2-3-Input AND-OR-INVERT Gate	MC501	MC551	MC401	MC451
SG60-63	Single 8-Input NAND Gate	MC502	MC552	MC402	MC452
SG90-93	2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement	MC503	MC553	MC403	MC453
SG100-103	Expandable 3-Wide 3-Input AND-OR-INVERT Gate	MC504	MC554	MC404	MC454
SG110-113	Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC505	MC555	MC405	MC455
SG120-123	Expandable 8-Input NAND Gate	MC506	MC556	MC406	MC456
SG130-133	Line Driver	MC507	MC557	MC407	MC457
SG140-143	Quad 2-Input NAND Gate	MC508	MC558	MC408	MC458
SG150-153	4-Wide 3-2-2-3-Input Expander for AND-OR-INVERT Gates	MC509	MC559	MC409	MC459
SG170-173	Dual 4-Input Expander for AND-OR-INVERT Gates	MC510	MC560	MC410	MC460
SG180-183	Dual 4-Input Expander for NAND Gates	MC511	MC561	MC411	MC461
SG190-193	Triple 3-Input NAND Gate	MC512	MC562	MC412	MC462
SF10-13	R-S Flip-Flop	MC513	MC563	MC413	MC463
SF50-53	AND J-K Flip-Flop	MC515	MC565	MC415	MC465
SF60-63	OR J-K Flip-Flop	MC516	MC566	MC416	MC466
SG70-73	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC520	MC570	MC420	MC470

^{*}Trademark of Motorola Inc. †Trademark of Sylvania Electric Products, Inc.



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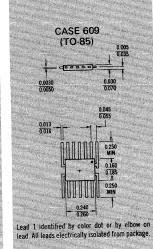
DEFINITIONS

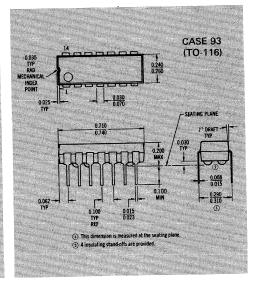
BVin "0"	Input breakdown voltage (ON level)
BVin "t"	Input breakdown voltage (OFF level)
CT	Total parasitic capacitance, which includes probe, wiring, and load capacitances
fTog	Toggle frequency
hFE	Forward beta
1 _{B1} , 1 _{B2}	Base current
Ic .	Collector Current
IF The second	Input forward current
lin .	Input current
II	Inverse beta current
Imax	Maximum rated power supply current with V _{max} applied
lo .	Output breakdown current
Тон	Output high current
IOL	Output low current
OLK	Output leakage current
ІРОН	Power supply drain with inputs high
IPDL	Power supply drain with inputs low
I _R	Input reverse current with VR applied
Isc	Short circuit current obtained from device output when one or more inputs are low
Pr	Prime fan-out
PRF	Pulse repetition frequency
PW	Pulse width
RG	Generator resistance
RL	Load resistance
Std	Standard fan-out
tf	Fall time
toff	Turn-off delay time
ton	Turn-on delay time
tpost	The minimal time necessary before the SET, PRESET or RESET inputs can control the flip-flop after the negative clock edge

tr	Rise time
Δtpd	Average increase in propagation delay per AND gate of expander when connected to an AND-OR-INVERT gate
Δt _{pd} /pF	Increased propagation delay caused by additional capacitance at expansion points
TPin	Test point at input of device under test
TPout	Test point at output of device under test
VAmp	Voltage amplitude
V _{BC}	Base-collector voltage
VBE	Base-emitter voltage
Ve	Collector voltage
Vcc	Power supply voltage
Vcch	High power supply voltage
VCE.	Collector-emitter voltage
VCR	Collector voltage obtained thru 1.3 k ohm resistor from VCC
VCRH	Collector voltage obtained thru 1.3 k ohm resistor from VCCH
VDC	Voltage obtained with two series diodes tied from collector to ground
V _{E1} , V _{E2} , V _{E3}	Emitter voltage
VEN	Enable voltage level
ViH	Voltage for high input voltage state
VIHX	Reduced supply voltage to hold input above thres- hold and to prevent noise from entering the device
VIL	Voltage for low input voltage state
VINH	Inhibit voltage level
V _{max}	Maximum rated power supply voltage (VCC)
Vo	Offset voltage
.о Уон	Output high voltage with IOH flowing out of pin
VOL	Output low voltage with IOL flowing into pin
Vout	Output voltage
Vout "0"	Output low voltage with Vth "1" applied
Vout "1"	Output high voltage with Vth "0" applied
VR	Input reverse voltage
V _{th} "0"	Logic "0" threshold voltage
V _{th} "1"	Logic "1" threshold voltage

PACKAGING

All MTTL integrated circuits are available in the TO-85, 14-lead flat package, MC400 series is also available in the 14-lead dual in-line plastic package. To order the flat package, add suffix "F" to the basic type number; to order plastic package, add suffix "P".

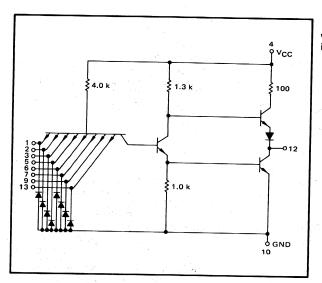




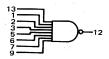
SINGLE 8-INPUT "NAND" GATE

MTTL MC500/400 series

MC502 · MC552 MC402 · MC452



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders or decoders.

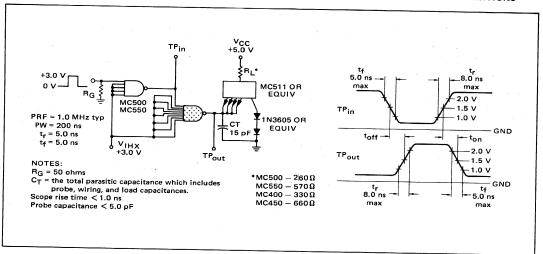


Positive Logic: 12 = 1 • 2 • 3 • 5 • 6 • 7 • 9 • 13 Negative Logic: 12 = 1 + 2 + 3 + 5 + 6 + 7 + 9 + 13

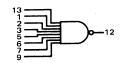
Total Power Dissipation = 15 mW typ/pkg Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	41.1			
	THE ST ESTABILITY TACTOR	(1F)	OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC502 MC552	1	(-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC402 MC452	1	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUITS



Test procedures are shown for only one input of the gate. To complete testing, sequence through remaining inputs in the same manner.



							TEST CONDITIONS									
				mA			Volts									
	@ Test I _{OL} I _{OH}							V _{IH}	V _R	V _{th 1}	V _{th 0}	٧	V _{cc}	V _{cch}	V _{IHX}	
Temperature		Pr*	Std	Pr*	Std	lin	٧ _{١L}	· IH	"R	"th 1	*th O	* out	•cc	, CCH	TIHX	
- J	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0		-	
MC502*, MC552	+25℃	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	1.7	1.2	5.5	5, 0	8.0	3.0	
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5, 0	-	-	
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-	
MC402*, MC452	{ +25℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0	
	(+75℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0			
MCAES Took Limite		l								-						

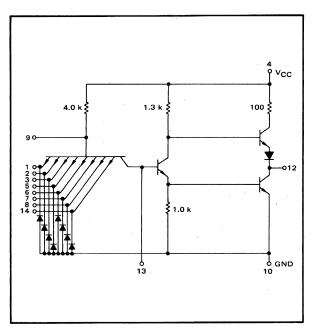
														(+75°C	20 10	-1.2 -0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-	
		Pin		1C502,								52 Te					TEST CURI	RENT	/ VOLT	AGE A	PPLIED	TO P	INS LI	STED	BELOW	l :		
		Under		55°C		25°C		25°C)°C		25°C	_	′5°C		-												┨ .
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	l _{ОН}	lin	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	V _{CCH}	V _{IHX}	Gnd
Input	T	T		Τ	Γ -	Г				Γ	Γ				Τ	T	T	Г			Γ		Г	Γ				
Forward Current	$I_{\mathbf{F}}$	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3,5,6, 7,9,13	-	-	-	4	-	-	1,10
Leakage Current	I _R	1	-	100	1	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 9,10,13
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV in ''0''	1	-	-	-	5.5	-	-	-	Ι-	-	5.5	-	-	Vdc	-	-	1	-,	-	-	-	-	T -	4	-	1	10
e e e	BV _{in"1"}	1		-	-	5.5	-	-	-	-	-	5.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 9,10,13
Output Output Voltage	v	12	T_	0.45	_	0. 45		0.45	_	0.45	_	0.45		0, 45	Vdc	12		_		_		1	_	_	4	_		10
Output Voltage	V _{out ''0''}	12	2.5	0.40	2.4	0.40	2.7	0.40	2.5	0.40	2. 4	0.40	2.5	0. 40	Vdc	-	12	-	<u> </u>			<u> </u>	1	+-	4			10
	Vout "1"						-		<u> </u>			ļ.,,		050	μAdc					-			-	12	4	-		1,2,3,5,6,
Leakage Current	IOLK	12	-	250	-	250	_	250	-	250	-	250	-	250	μΑαс	-	_	_	-	-	_	-	_	12	4		-	7,9,10,13
Short-Circuit Current	I _{SC}	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAde	-	-	-	-	-	-	-	-	-	4	-		1,2,3,5,6, 7,9,10,13
Output Voltage	V _{OL}	12	-	0.40	-	0.40	-	0.45	T	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	-	10
	v _{OH}	12	2.8	-	3.2	-	3.35	-	3.0	-	3. 1		3. 15	-	Vdc	-	12	-	1	-	-	-	-	-	4	-		10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	- '.	-	-	-	-	4	-	1,10
Power Supply Drain	I _{PDH}	4	-	6.0	-	6.0	-	6.0	T-	7.5	-	7.5	-	7.5	mAdc	-	-	-	-	-	-	-	-	-	4	-	- 1	10
	I _{PDL}	4	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	3, 0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,10
Switching Parameters																Pulse In	Pulse Out										5	
Turn-On Delay	ton	1,12	-	-	-	24	-	-	-	-	-	24	-	-	ns	1	12	-	-		-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Turn-Off Delay	toff	1,12	-	Γ-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4		2,3,5,6, 7,9,13	10
Rise Time	t _r	1,12	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Fall Time	t _f	1, 12	-	-	-	5.0	- 7	-	-	-	-	5.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10

^{*}Prime Fan-Out.

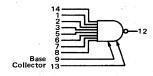
EXPANDABLE 8-INPUT "NAND" GATE

MTTL MC500/400 series

MC506 · MC556 MC406 · MC456



This device consists of an 8-input AND gate driving an output inverter. The base and the collector of the multiple emitter input transistor are available as expander terminals. The number of inputs can be expanded to 20 by using the MC511 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.

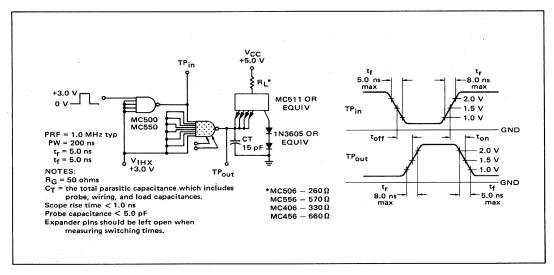


Positive Logic: 12 = 1 • 2 • 3 • 5 • 6 • 7 • 8 • 14 • Expanders Negative Logic: 12 = 1 + 2 + 3 + 5 + 6 + 7 + 8 + 14 + Expanders

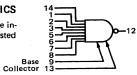
Total Power Dissipation = 15 mW typ/pkg Propagation Delay Time = 18 ns typ

SERIES	INPUT LOADING FACTOR	(I _F)	OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC506 MC556	1	(1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC406 MC456	1	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the gate. The other inputs are tested in the same manner.



							TE	ST CO	NDITIO	NS							
				mA			Volts										
	@ Test	ار	DL .	I _C	н	l _{in}	I _{in} V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	V _{ccH}	V _{IHX}		
Temperature		Pr*	Std	Pr*	Std	į.	A II	* IH	*R	- th 1	"th O	out	*cc	*ссн	*IHX		
	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	2.0	1.0	5.5	5.0		-		
MC506*, MC556	425℃	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0		
	(+125℃	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-		
	(°°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-		
MC406*, MC456	{ +25℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0		
	(+75℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-		
ACATA T A 12 's																	

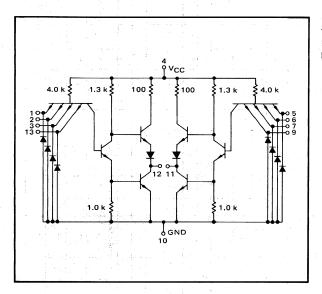
														(+75℃	20 10	-1.2 -0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-	
		Pin		MC506	,					AC406							TEST CURF	RENT	/ VOLT	AGE A	APPLIED	TO P	INS-LI	STED	BELOW	':		
Characteristic	Symbol	Under Test	Min	55°C Max		25°C Max		25°C Max		°C Max		25°C Max		5°C Max	Unit	lou	I _{OH}	l _{in}	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th O}	V _{out}	V _{cc}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _F	1	-	-1. 33	-	-1. 33	-	-1. 33	-	-1.66	-	-1. 66	-	-1.66	m Adc	-	_	-	-	-	2,3,5,6, 7,8,14	-	-	-	4	-	-	1,10
Leakage Current	IR	1	-	100	-	100	-	100	-	100	-	100	-	100	μ Adc	-	-	-	-	-	1	-	-	-	4	-		2,3,5,6,7, 8,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μ Adc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV in "0"	1	5.5	-	5. 5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-		1	-	-	-	-	-	-	4	-	-	10
	BV _{in"1"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5. 5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 8,10,14
Output Output Voltage	v _{out "0"}	12	Ι-	0.45	-	0. 45	-	0.45	-	0. 45	-	0. 45	-	0. 45	Vdc	12	-	-	-	-	-	1	-	-	4	-	-	10
	v _{out ''1''}	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	IOLK	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6, 7,8,10,14
Short-Circuit Current	I _{SC}	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7 8,10,12,14
Output Voltage	v _{ol}	12	Ι-	0.40		0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1		-	-	-	4	-	-	10
	V _{OH}	12	2.8	-	3. 2	- T	3. 35	-	3.0	-	3.1	-	3. 15		Vdc		12	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	<u>-</u>	-	-	-	-	-	-	-	-	4	-	1,10
Power Supply Drain	I _{PDH}	4	-	6.0	-	6.0	-	6.0	-	7.5	-	7.5	-	7.5	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10
	IPDL	4	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,10
Switching Parameters Turn-On Delay	, ton†	1,12	-	-	-	28	-	:-	-	-	-	28	-	-	ns	Pulse in	Pulse Out	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,8,14	10
Turn-Off Delay	toff	1,12	-		F	20	-	-		-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6 7,8,14	10
Rise Time	t _r	1,12	-		-	8.0	-	-	-		-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6 7,8,14	10
Fall Time	t _f	1,12	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6 7,8,14	10

^{*} Prime Fan-Out.
† Add 3.0 ns for each AND expander (1/2 MC511, MC561, MC411, and MC461) used.
Add 2.0 ns t_{pd} for each pF added to either expander points.

DUAL 4-INPUT "NAND" GATE

MTTL MC500/400 series

MC500 · MC550 MC400 · MC450



This device consists of two 4-input NAND gates. The gates can be cross-coupled to form a multiple-input R-S flip-flop or a circuit for eliminating contact bounce.

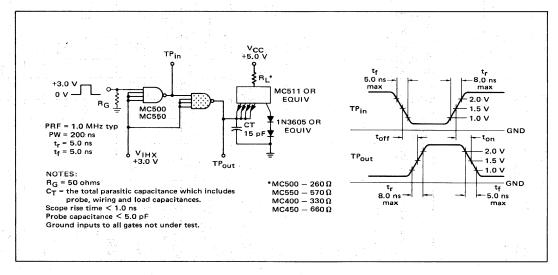


Positive Logic: $12 = 1 \cdot 2 \cdot 3 \cdot 13$ Negative Logic: 12 = 1 + 2 + 3 + 13

Total Power Dissipation = 30 mW typ/pkg Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR (IF)	OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC500 MC550	1 (-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC400 MC450	1 (-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



			-				TI	ST CO	NDITIO	NS					
				mA							Volts				
	@ Test	ار	DL	ار	ЭН		v	v	v	v	v	v	V	V	V
Ter	nperature	Pr*	Std	Pr*	Std	'in	VIL	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	V _{CCH}	V _{IHX}
	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
MC500*, MC550	{ +25℃	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	(+125℃	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0, 9	5,5	5.0	-	-
,	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4. 5	1.9	1.1	5.5	5.0	-	-
MC400*, MC450	{ +25℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-
MC450 Test Limits															

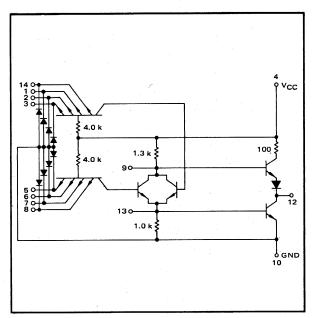
		Pin				50 Te				C400,			st Lin	nits		\\	TEST CURI	RENT	/ VOLT	AGE A	APPLIED	TO P	INS L	STED	BELOW) :		1
		Under		5°C		25°C		25°C		°C		25°C		′5°C] .							·						1
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	OL	Іон	lin	V _{IL}	V _{IH}	V _R	V _{th} 1	Vtho	Vout	V _{cc}	V _{ccн}	V _{IHX}	Gnd †
Input Forward Current	I _F	1	-	-1.33	-	-1. 33	-	-1. 33	-	-1. 66	-	-1. 66	-	-1.66	mAdc	-	-	-	-	-	2,3,13	-	-	-	4	-	-	1,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10,13
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	. 1	-		7-	4	-	-	10
Breakdown Voltage	BV in ''0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-		-	-	-	4	-	-	10
	BV _{in"1"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10,13
Output Output Voltage	V _{out "0"}	12	-	0. 45	-	0.45	-	0.45	-	0.45	-	0.45	-	0. 45	Vdc	12	-	-	-	-	_	1	-	-	4	-	-	10
	v _{out "1"}	12	2.5	-	2.4	-	2.7	-	2. 5	-	2. 4	-	2.5	T-	Vdc	-	12	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	IOLK	12	- 1	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3, 10,13
Short-Circuit Current	I_{SC}	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	J. 3	1,2,3, 10, 12, 13
Output Voltage	v _{OL}	12	- "	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-		1	-	-	-	-	4	-	-	10
	V _{ОН}	12	2.8	-	3.2	-	3.35	-	3.0	-	3. 1	-	3. 15	-	Vdc	-	12	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	. -	10	-	- - -	-	-	-	10	-	-	mAde	-	-	-	-	-	-	_	-	-	-	- 4	- -	1,5,10
Power Supply Drain	I _{PDH}	4	-	12	-	12	-	12	-	15	-	15	-	15	mAdc	-	-	-	-	-	-	-	T -	-	4	-	- ,	10‡
	I_{PDL}	4	-	6.0		6.0		6.0	-	6.0	-	6.0	-	6.0	mAde	-	-	-	-	-	-	-	-	-	4	-	-	1,5,10
Switching Parameters Turn-On Delay	ton	1,12	-	-	-	20	-		-	_		20	-	-	ns	Pulse In	Pulse Out	_	-	-	-	_	-	-	4		2,3,13	10
Turn-Off Delay	toff	1,12	-	-	-	20	-	-	-	-	-	20	-	-	ns.	1	12	-	-	-	-	-	† -	† - ·	4	; -	2,3,13	10
Rise Time	tr	1,12	-	-	-	8.0	-	-	-	-		8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	2 -	2,3,13	10
Fall Time	t _f	1,12	-	-	-	5.0	-	-	-	- :		5.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,13	10

[†] Ground inputs to gates not under test during ALL tests, unless otherwise noted. ‡ The inputs of all gates must be ungrounded.

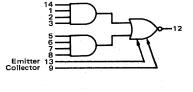
EXPANDABLE 2-WIDE 4-INPUT "AND-OR-INVERT" GATE

MTTL MC500/400 series

MC505 · MC555 MC405 · MC455



This device consists of two 4-input AND gates ORed together and driving an output inverter. The ORing nodes are available for expansion and up to 10 AND gates can be ORed together using the MC509 or MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds

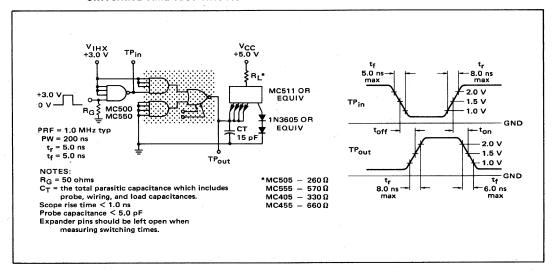


Positive Logic: 12 = (1 • 2 • 3 • 14) + (5 • 6 • 7 • 8) + (Expanders) Negative Logic: 12 = (1 + 2 + 3 + 14) • (5 + 6 + 7 + 8) • (Expanders)

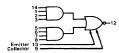
Total Power Dissipation = 20 mW typ/pkg Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(IF)		OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC505 MC555	1	(-1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC400 MC450	1	(-1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the device. To complete testing sequence through remaining inputs in the same manner.



							TE	ST CO	NDITIO	NS					
				mÆ							Volts				
	@ Test	l _c)L	Ic	Н		V _{IL}	V _{IH}	V _R	V _{th 1}	v	v	V _{cc}	v	V _{IHX}
Ten	perature	Pr*	Std	Pr*	Std	l _{in}	¥ IL	*ін	*R	With 1	V _{th 0}	Vout	*cc	V _{CCH}	* IHX
	—55°C	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	2. 0	1.0	5.5	5.0	-	-
MC505*, MC555	+25℃	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0		-
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
MC405*, MC455	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	

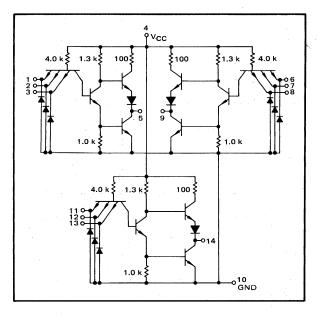
														(+75°C	20 10	-1.2 -0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-	
		Pin		MC505						NC405							TEST CURI	RENT	/ VOLT	AGE A	APPLIED	TO P	INS L	STED	BELOV	/ :		1
		Under		55°C		25°C		25°C)°C		25°C		75°C	l	<u> </u>	T .	Γ.	·			,						1
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	I _{ОН}	1 in	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	$\mathbf{I}_{\mathbf{F}}$	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3,14	-	-	-	4	-	-	1,5,6,7, 8,10
Leakage Current	IR	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 8,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	5,6,7,8,10
Breakdown Voltage	BV _{in ''0''}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-		-	-	4	-	-	5,6,7,8,10
	BV _{in ''1''}	1	5.5	-	5. 5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-		1	-	-	-		-	-	4	-	-	2,3,5,6,7, 8,10,14
Output Output Voltage	v _{out ''0''}	12	_	0. 45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	T -	4	-	-	5,6,7,8,10
	Vout "1"	12	2.5	-	2.4	T =	2.7		2.5	-	2.4	† -	2.5	†-	Vdc	-	12	-	-	-	-	-	1	†=	4	-	-	5,6,7,8,10
Leakage Current	IOLK	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6, 7,8,10,14
Short-Circuit Current	I _{SC}	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,8,10, 12,14
Output Voltage	V _{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	† - -	† -	4	-	-	5,6,7,8,10
	V _{OH}	12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3. 15	-	Vdc	-	12	-	1	-	-	1	-	-	4	-	-	5,6,7,8,10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	_	4	-	1,2,3,5,6, 7,8,10,14
Power Supply Drain	I _{PDH}	4	-	7.0	-	7.0	-	7.0	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	-	T -	4	-	-	10
	I _{PDL}	4	-	4.0	-	4.0	-	4.0	-	4.0	-	4.0	-	4.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,8,10,14
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	ton	1,12	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Turn-Off Delay	t _{off}	1,12	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	12	-	- '	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Rise Time	t _r	1,12	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Fall Time	t _f	1,12	-	-	-	6.0	-	-		-	-	6.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10

^{*} Prime Fan-Out

TRIPLE 3-INPUT "NAND" GATE

MTTL MC500/400 series

MC512 · MC562 MC412 · MC462



This device consists of a 3-input AND gate driving an output inverter. This gate can be used to build a pulse shaping network for interfacing with discrete component circuits.

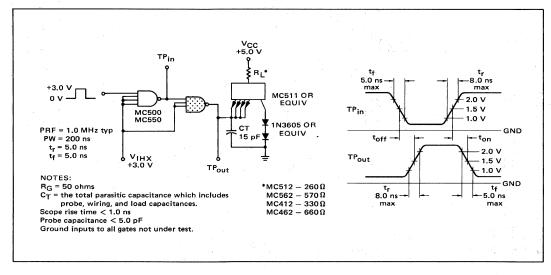


Positive Logic: $5 = \overline{1 \cdot 2 \cdot 3}$ Negative Logic: $5 = \overline{1 + 2 + 3}$

Total Power Dissipation = 45 mW typ/pkg Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR	(IF)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC512 MC562	1	(-1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC412 MC462	1	(-1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



							TE	ST CO	NDITIO	NS	1				
				mA							Volts				
(@ Test	ار	DL .	ار	Н		VIL	V _{IH}	V _R	V _{th} 1	V _{th 0}	V _{out}	٧ _{cc}	V _{cch}	V _{IHX}
Ter	nperature	Pr*	Std	Pr*	Std	lin	*IL	۲ін	*R	*th 1	*th 0	out	· C	*ссн	TIHX
	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	2.0	1.0	5.5	5.0	-	٠-
MC512*, MC562	{ +25℃	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	(+125℃	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
MC412*, MC462	} +25℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1. 2	5.5	5.0	7.0	3. 0
	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

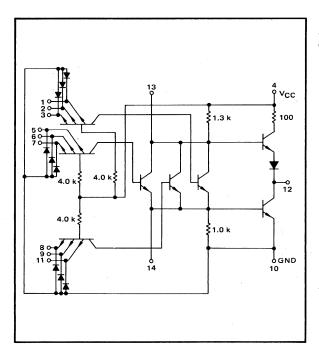
															173 C	20 10	-1. 2 -0.0	1.0	0, 10	0.0	4.0	1.1.	1.1	0.0	0.0			
		Pin	_		<u>. </u>	562 Te				1C412,							TEST CURI	RENT	/ VOLT	AGE A	PPLIED	TO P	INS LI	STED	BELOW	/:		
Characteristic	Symbol	Under Test		55°C Max		25°C Max		25°C Max		°C Max		25°C Max		5°C Max	Unit	l _{ol}	Гон	l _{in}	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th O}	V _{out}	٧ _{cc}	V _{CCH}	V _{IHX}	Gnd †
In-out	T		1	1	_		T	T		ī -					г -	T	T					T -	T		_			
Input Forward Current	I _F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3		-	-	4	-	-	1,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	T -	100	μAdc		-	-	-	-	1	-	-	-	4	-		2,3,10
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-		-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV _{in "0"}	1	5.5	-	5. 5	-	5.5	-	5.5		5. 5	-	5.5	-	Vdc	÷	-	1	-	-	- '	_	-	-	4	-	-	10
	BV _{in "1"}	1	5.5	T - '	5.5	-	5.5	-	5.5	-	5. 5	-	5.5	-	Vdc	-		1	-	-	- ,		-	-	4	-	-	2,3,10
Output Output Voltage	v _{out "0"}	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0. 45	Vdc	5	-	-	-	_	-	1	-	-	4	-	-	10
	Vout "1"	5	2.5	-	2.4	-	2.7	-	2.5	-	2.4	1	2.5	-	Vdc	-	5	-	-	-	- ,	-	1	-	4	-	-	10
Leakage Current	IOLK	5	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	5	4	-	-	1,2,3,10
Short-Circuit Current	I _{SC}	5	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3, 5,10
Output Voltage	V _{OL}	5	-	0.40	-	0.40	- 1	0.45	-	0.40	-	0.40	-	0.45	Vdc	5	-	-	-	1		-	-	-	4	-	-	10
	V _{OH}	5	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	5	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	_	- -	15	-	-	-	-		15		-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,6,10,11
Power Supply Drain	I _{PDH}	4	-	18	-	18	-	18	-	22.5	-	22.5	-	22.5	mAdc	-	-	l -	-	-	-	Γ-	-		4	-	-	10 ‡
	I _{PDL}	4	T -	9.0	-	9.0	-	9.0	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	1	1,6,10,11
Switching Parameters																Pulse In	Pulse Out				-				4	_	2,3	10
Turn-On Delay	ton	1,5	<u> </u>			20		-	-	ļ-	Ŀ	20	<u> </u>		ns	1	5	-		-	-	<u> </u>	-	-	4		2,3	10
Turn-Off Delay	toff	1,5	<u> </u>	-		8.0	<u> </u>		-	<u> </u>	<u> </u>	8.0	-	-	L	1	5	-	<u> </u>	-	<u> </u>	⊢ <u>-</u> -	H	H	4	<u> </u>	2,3	10
Rise Time	t _r	1,5	ļ -	<u> </u>			<u> </u>				<u> </u>	5.0	<u> </u>		ns ns	1	5	-		_	<u> </u>	 - -		- -	4	<u> </u>	2,3	10
Fall Time	t _f	1,5	-	-	-	5.0			-	1 -	-	3.0	- I		ns	1	3	_					L -	L	-4		2,0	10

^{*} Prime Fan-Out † Ground inputs to gates not under test, during ALL tests unless otherwise noted. ‡ The inputs to all gates must be ungrounded.

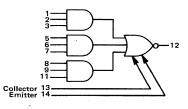
EXPANDABLE 3-WIDE 3-INPUT "AND-OR-INVERT" GATE

MTTL MC500/400 series

MC504 · MC554 MC404 · MC454



This device consists of three 3-input AND gates ORed together driving an output inverter. The common ORing nodes are available for expansion, and up to 10 AND gates can be ORed together using the MC509 or the MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

12 = (1 • 2 • 3) + (5 • 6 • 7) + (8 • 9 • 11) + (Expanders)

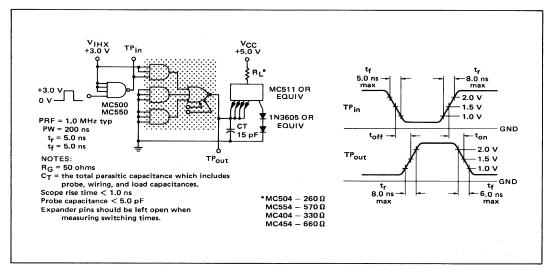
Negative Logic:

 $12 = \overline{(1+2+3) \cdot (5+6+7) \cdot (8+9+11) \cdot (Expanders)}$

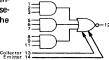
Total Power Dissipation = 25 mW typ/pkg Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(1 _F)		OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC504 MC554	1	(-1.33 mA)		MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC404 MC454	1	(-1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the device. To complete testing sequence through remaining inputs in the same manner.



	② Tes
AC504*, MC554	+2 +2

@ Test
Temperature
/ 55%

- 1			mΑ							Volts				
st	ار)L	Ic	Н		VIL	V _{IH}	V _R	v	٧	٧	v	V _{ccH}	V _{IHX}
ure	Pr*	Std	Pr*	Std	lin	¥ IL	* ін	*R	Tth 1	* th O	V out	*cc	*ссн	* IHX
°c	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
°c	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
°c	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	
)°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	
5°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
5°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

TEST CONDITIONS

	MC404	٠,	MC454
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MC404*,	MC454	{	

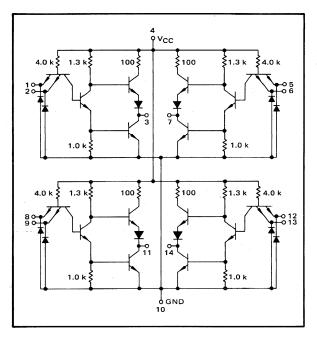
	l	Pin	٨	AC504	, MC	554 Te	st Lin	nits		IC404,							TEST CURF	RENT	/ VOLT	AGE A	APPLIED	TO P	INS LI	STED	BELOW	V :		
		Under		55°C		25°C		25°C		°C		25°C		5°C		1										_	v	ا بـــ
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	Іон	lin	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	V _{ccн}	V _{IHX}	Gnd
Input Forward Current	I _F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3	-	-	-	4	-		1,5,6,7,8, 9,10,11
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μ Ad c	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 8,9,10,11
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μ Ad c	-	-	-	-	-	1	-	- '	<u> </u>	4	-	-	5,6,7,8,9, 10,11
Breakdown Voltage	BV in "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	<u> </u>	-	4		-	5,6,7,8,9, 10,11
	вv _{in ''1''}	1	5.5	-	5. 5	-	5. 5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 8,9,10,11
Output Output Voltage	v _{out "0"}	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	-	4	-	-	5,6,7,8,9, 10,11
	v _{out "1"}	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	-	4	-	-	5,6,7,8,9, 10,11
Leakage Current	IOLK	12	-	250	-	250	-	250	-	250	-	250	-	250	μ Adc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6, 7,8,9, 10,11
Short-Circuit Current	I _{SC}	'12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-		-	-	-	-	4	-	-	1,2,3,5,6, 7,8,9,10, 11,12
Output Voltage	V _{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	-	5,6,7,8,9, 10,11
	V _{ОН}	12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	•	12	-	1	-	-	-	-	<u> </u>	4	-	-	5,6,7,8,9, 10,11
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	10	-	-	-	-	-	10	-	-	mAde	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6, 7,8,9, 10,11
Power Supply Drain	I _{PDH}	4	T -	8.0	-	8.0	-	8.0	-	10	-	10	-	10	mAdc	-	-	-	-	-		-	-	-	4	<u> </u>	-	10
	IPDL	4	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,8,9, 10,11
Switching Parameters	 	 	+-	_	—	 	_	1	T	1	\vdash	 -	1	†	-	Pulse In	Pulse Out	T	 	<u> </u>			\vdash	T				
Turn-On Delay	ton	1,12	-	-	-	22	-	_	-	-	-	22	-	-	ns	1	12	1-	-	-	-	-	-	-	4	-	2,3	5,6,7,8,9, 10,11
Turn-Off Delay	toff	1,12	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3	5,6,7,8,9, 10,11
Rise Time	t _r	1,12	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3	5,6,7,8,9, 10,11
Fall Time	t _f	1,12	Γ-	-	-	6.0	-	-	-	-	-	6.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3	5,6,7,8,9, 10,11

^{*} Prime Fan-Out

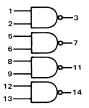
MTTL MC500/400 series

QUAD 2-INPUT "NAND" GATE

MC508 · MC558 MC408 · MC458



This device consists of four 2-input NAND gates. The four gates in a single package represent increased functional flexibility. For example, a dual set-reset flipflop may be obtained if each pair of gates is externally cross-coupled.

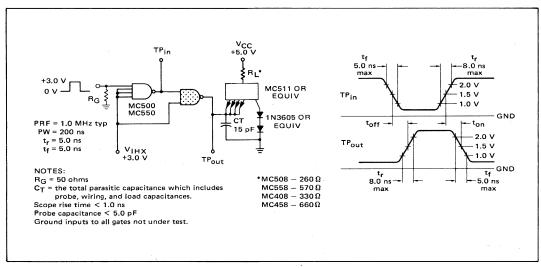


Positive Logic: $3 = 1 \cdot 2$ Negative Logic: 3 = 1 + 2

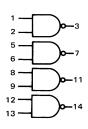
Total Power Dissipation = 60 mW typ/pkg Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR	(IF)	OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC508 MC558	1	(-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC408 MC458	1	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0 ^o to +75 ^o C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. The other input is tested in the same manner.



							TE	ST CO	NDITIO	NS					
				mA							Volts				
(@ Test	ار)L	ار	Н		V	V	v	v	v	V	v	V	v
Ter	nperature	Pr*	Std	Pr*	Std	'in	٧	VIH	V _R	Vth 1	V th O	Vout	*cc	V _{CCH}	V _{IHX}
	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
AC508*, MC558	+25°C	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0		-
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
AC408*, MC458	{ +25℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5. 5	5.0		-
CASO Tact Limite															

		Pin		AC508						1C408,							TEST CURI	RENT	/ VOLT	AGE A	PPLIED	TO P	INS LI	STED I	BELOW	· :		1
Characteristic	Symbol	Under Test		55°C Max		25°C Max		25°C Max	Min)°C		25°C Max		′5°C	Unit	lor	l _{oн}	lin	٧٫٫		V _R	V _{th 1}		,	V _{cc}	V _{CCH}	V _{IHX}	Gnd†
Citatacteristic	Зуньон	1631	MILL	IVIdX	MILL	INGX	IAMI	IVIGA	IAMII	MIGA	MILL	MIGX	MILLI	MIGX	Oilli	OL.	OH	_ in		· III		Th I.	mo	OUT		CCH		- Ond 1
Input Forward Current	I _F	1	-	-1. 33	-	-1. 33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2	-	-	-	4	-	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,10
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV _{in"0"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5. 5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	10
	BV _{in"1"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,10
Output Output Voltage	v _{out} ₀	3	-	0.45	-	0.45	-	0.45	-	0.45	-	0. 45	_	0.45	Vdc	3	-	-	-	_	-	1	_	-	4	-	-	10
	Vout "1"	3	2. 5	-	2. 4	-	2. 7	-	2.5	-	2.4	-	2. 5	-	Vdc	-	3	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	IOLK	3	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	3	4	-	-	1,2,10
Short-Circuit Current	I _{SC}	3	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10
Output Voltage	V _{OL}	3	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	3	-	-	-	1	-	-	-	-	4	-	-	10
	V _{OH}	3	2.8	-	3. 2	-	3.35	-	3.0	-	3. 1	-	3. 15	-	Vdc	-	3	-	1	-	-	-	Ι-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	20	-	-	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4		1,5,8,10,12
Power Supply Drain	I _{PDH}	4	-	24	-	24	-	24	-	30	-	30	-	30	mAde	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	IPDL	4	-	12	-	12	-	12	-	12	-	12	-	12	m Adc	-	-	-	-	-	-	-	T-	-	4	-	-	1,5,8,10,12
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	ton	1,3	-	-	-	20	-	-		_	-	20	Ŀ	-	ns	1	3		-	-	-	-	-	-	4	-	2	10
Turn-Off Delay	toff	1,3	-	_	-	20	-	-	_	Ε-	-	20		-	ns	1	3	-	-	-	-	-		-	4	-	2	10
Rise Time	tr	1, 3	-		-	8.0	-	-	_	-	-	8.0	<u> </u>	-	ns	1	3	-	-	-	-		Ŀ	-	4	-	2	10
Fall Time	t _f	1,3	-	-	-	5.0	-	γ5 <u>-</u>	-	-	-	5.0	-	-	ns	1.	3	-	-	-	-	-	-	-	4	-	2	10

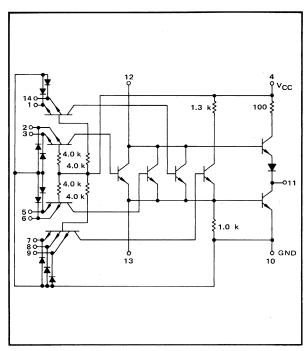
^{*} Prime Fan-Out.

[†] Ground inputs to gates not under test, during ALL tests unless otherwise noted. ‡ The inputs to all gates must be ungrounded.

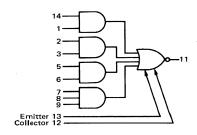
EXPANDABLE 4-WIDE 2-2-2-3 INPUT "AND-OR-INVERT" GATE

MTTL MC500/400 series

MC501 · MC551 MC401 · MC451



This device consists of three 2-input and one 3-input AND gates internally ORed together and then inverted to provide the output. The common ORing nodes are available for expansion and up to 10 AND gates can be ORed together using the MC509 and the MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

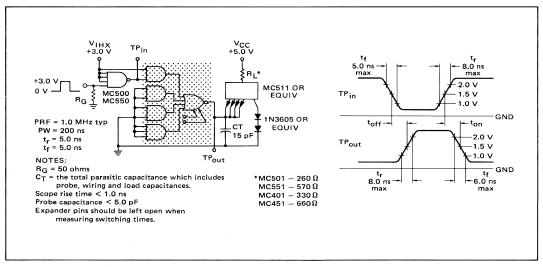
11 = (14 • 1) + (2 • 3) + (5 • 6) + (7 • 8 • 9) + (Expanders)
Negative Logic:

 $11 = \overline{(14+1) \cdot (2+3) \cdot (5+6) \cdot (7+8+9)} \cdot (Expanders)$

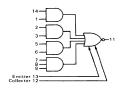
Total Power Dissipation = 30 mW typ/pkg Propagation Delay Time = 12 ns typ

ĺ	SERIES	INPUT LOADING FACTOR	(IE)	OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
	MC501 MC551	1	(-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
	MC401 MC451	1	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0º to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for one input of the device. To complete testing, sequence through remaining inputs in a similar manner.



							TE	ST CO	NDITIO	NS					
				mΑ							Volts				
(② Test	I,	DL	ار	ЭН	l _{in}	VIL	V _{IH}	V _R	V _{th} 1	V _{th 0}	Vout	۷ _{cc}	V _{ccH}	V _{IHX}
Tem	perature	Pr*	Std	Pr*	Std	'in	* IL	* IH	*R	'th 1	* th O	* out	'CC	'ссн	·IHX
(_55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
MC501*, MC551	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
(+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
MC401*, MC451	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

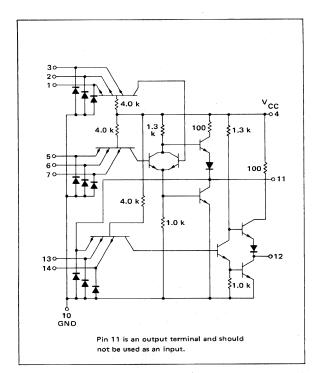
											ig.c	, ,	1110-10	- 1	+75°C	-	10	-1.2 -0.6		0.45	_	4.5	1.7	 	5.5	5.0		0.0	1
	Γ	Pin		AC501	MC!	551 Te	st lin	nits	١ ٨	AC401	MC4	151 Te	st Lin		1/3 C	20	10	TEST CURR					-			ı	,		1
		Under	1	55°C		25°C		25°C)°C		25°C		′5°C	1			IEST CORK	ENI	/ VULI	AGE A	APPLIED	,		,	BELOW	l :		1
Characteristic	Symbol	Test	-			Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor		I _{OH}	l _{in}	VIL	ViH	V _R	V _{th 1}	V _{th O}	Vout	۷ _{cc}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	m Ade	-		-	-	-	-	14	-	-	-	4	-	-	1,2,3,5,6,7 8,9,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-		-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7,8 9,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-		-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 8,9,10
Breakdown Voltage	BV _{in''0''}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-		-	1	-	-	-	-	-	-	4	-	-	2,3,5,6, 7, 8, 9, 10
	BV _{in"1"}	1	5.5	-	5. 5	-	5. 5	-	5. 5	-	5. 5	-	5. 5	-	Vdc	-		-	1	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,8,9,10,14
Output Output Voltage	v _{out "0"}	11	-	0. 45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11		-	-	-	-	-	1	-	-	4		-	2,3,5,6,7, 8,9,10
	v _{out "1"}	11	2.5	-	2. 4	-	2. 7	-	2.5	-	2. 4	-	2.5	-	Vdc	-		11	-	-	-	-	-	1	-	4	-	-	2,3,5,6,7. 8,9,10
Leakage Current	I _{OLK}	11	-	250	-	250	-	250	-	250	-	250	-	250	μ A dc	-		-	-	-	-	-	-	-	11	4	-	-	1,2.3,5,6,7 8,9,10,14
Short-Circuit Current	I _{SC}	11	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-		-	-	-	-	-	-	-	-	4	-	-	1, 2, 3, 5, 6 7,8,9, 10,11,14
Output Voltage	v _{OL}	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11		-	-	-	1	-	-	-	-	4	-	-	2,3,5,6,7. 8,9,10
	V _{ОН}	11	2.8	-	3. 2	-	3. 35	-	3.0	-	3. 1	-	3. 15	-	Vdc	-		11	-	1	-	-	-	-	-	4	-	-	2,3,5,6,7, 8,9,10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	12	-	-	-	-	-	12	-	-	m Adc	-		-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6, 7,8,9,10,14
Power Supply Drain	I _{PDH}	4	T-	9.0	-	9.0	-	9.0	-	11	-	11	-	11	m Adc	-		-	-	-	-	-	-	-	-	4	-	-	10
	I _{PDL}	4	-	7.5	-	7.5	-	7.5	-	7.5	-	7.5	-	7.5	m Adc	-		-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,8,9,10,14
Switching Parameters		† • • • • • • • • • • • • • • • • • • •	†						 							Pulse	In	Pulse Out											
Turn-On Delay	ton	1,11	-	-	-	23	-	-	-	-	-	23	-	-	ns	1		11	-	-	-	-	-	-	-	4		14	2,3,5,6,7, 8,9,10
Turn-Off Delay	toff	1,11	-	-	-	23	-	-	-	-	-	23	-	-	ns	1		11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10
Rise Time	t _r	1,11	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1		11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10
Fall Time	t _e	1,11	-	† -	† -	6.0	-	-	-	-	-	6.0	-	-	ns	1		11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7,

^{*} Prime Fan-Out.

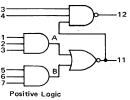
2-WIDE 3-INPUT "AND-OR-INVERT" GATE WITH GATED COMPLEMENT

MTTL MC500/400 series

MC503 · MC553 MC403 · MC453



This device is the only gate of the basic positive AND-OR-INVERT series that includes an additional 3-input AND-INVERT function on the output. This configuration provides the output and a gated complement in a single package. This device is useful in the design of adders, subtracters and one-shot multivibrators.



 $\begin{array}{r}
 11 = \overline{(1.2.3) + (5.6.7)} \\
 12 = \overline{11.13.14}
 \end{array}$

 $12 = (1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7) + \overline{13} + \overline{14}$

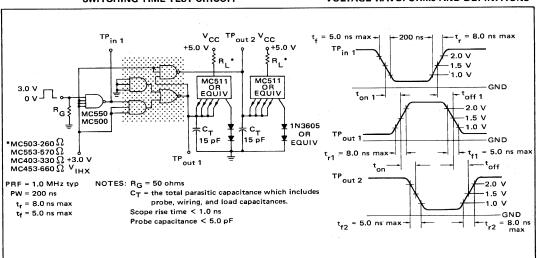
Total Power Dissipation = 35 mW typ/pkg
Propagation Delay Times = 11 ns typ (Pin 1 to Pin 11)
10 ns typ (Pin 11 to Pin 12)

TRUTH TABLE

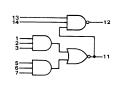
А	В	OUTPUT PIN # 11	PIN #13	PIN #14	OUTPUT PIN # 12
0	1	0	0	0	1
1	0	0	0	1	1
0	1	0	1	0	1 1
1	0	. 0	1	1	1
0	0	-1	0	0	1 1
0	0	1	0	1	1 1
0	0	1	1	0	1 1
0	0	1 .	1	1	0

SERIES	INPUT LOADING FACTOR (IF)	OUTPUT DRIVE (IC	DL) TEMPERATURE RANGE
MC503 MC553	1 (-1.33 mA)	15 MC500 Series Gates (20 7 MC500 Series Gates (10	-550C to +1250C
MC403 MC453	1 (-1.66 mA)	12 MC400 Series Gates (20 6 MC400 Series Gates (10	

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the AND-OR-INVERT gate, plus one input of the gated complement. To complete testing, sequence through remaining inputs in the same manner.



							T	ST CO	NDITIC	NS					
				mΑ							Volts				
(@ Test	٦	DL .	ار	ЭН		v	V	v	v	v	v	v	V	v
Ten	nperature	Pr*	Std	Pr*	Std	l _{in}	VIL	VIH	V _R	V _{th 1}	V _{th o}	V _{out}	V _{cc}	V _{CCH}	V _{IHX}
	_55°C	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	2.0	1.0	5.5	5.0	8.0	-
MC503*, MC553	+25℃	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	(+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	8.0	-
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	7.0	-
MC403*, MC453	{ +25℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4. 5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	7.0	-

															+75℃	20 10	-1.2 -0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	7.0	-	1 '
		Pin				553 T						53 Te:					TEST CUR	RENT	/ VOLT	TAGE A	APPLIED	TO P	INS II	STED	BELOW	· · · ·		1
el	١, , ,	Under		55°C		25°C		25°C)°C		25°C		′5°C		-	Τ.	Τ.			,		т -					-
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	Іон	lin	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th O}	Vout	Vcc	V _{CCH}	V _{IHX}	Gnd
Input					Г									Γ	1	l	Γ	Т		T	T	Т	F	T				
Forward Current	$^{\mathrm{I}}\mathrm{_{F}}$	1	-	-1.33	1	-1.33	1	-1.33	-	-1.66	1	-1.66	i		mAdc	-	-	-	-	-	2,3	-	-	-	4	-	-	1,5,6,7,10
		14	-	-1.33	-	-1.33	-	-1.33	ļ -	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	13	-	-	-	4	-	-	1,2,3,5,6, 7,10
Leakage Current	I _R	1	-	100	-	100	-	100 -	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	- 1	-	4	-	-	2,3,5,6, 7,10
		14	-	100	-	100	-	100	-	100	-	100	_	100	μAdc	_	-	-	-	_	14	_	_	-	4	_	_	10,13
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	†-	-	-	1	-	<u> </u>	† -	4	-	-	5,6,7,10
		14	-	100	-	100		100	-	100	-	100	-	100	μAdc	-	-	-	-	-	14	-	-	-	4	-	-	1,2,3,5,6, 7,10
Breakdown Voltage	BV _{in ''0''}	1	5. 5	-	5.5	-	5. 5		5. 5	-	5. 5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4			5,6,7,10
	ın o	14	5.5	-	5.5	-	5. 5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	14	-	-	-	-	-	-	4	-	-	1,2,3,5,6,
	BV _{in ''1''}	1	5.5	-	5.5	-	5.5	-	5.5	-	5. 5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-		2,3,5,6, 7,10
		14	5. 5	_	5.5	-	5.5	-	5.5	-	5.5	-	5. 5	-	Vdc	-	-	14	-	-	-	_	-	-	4	-	-	10,13
Output Output Voltage	v	11	Ι.	0.45		0. 45		0, 45		0.45		0.45	_	0.45	Vdc	11	_			_		1						5 0 7 10
Output Voltage	V _{out ''0''}	12	-	0.45	_	0.45	l _	0.45	_	0.45	I	0.45	-	0. 45	Vdc	12	_		-	1	_	14	-	-	4	-	-	5,6,7,10 1,2,3,5,6,
												0, 10										1		_	7	_	-	7,10
	v _{out ''1''}	11	2.5	-	2.4	-	2.7		2.5	ŀ	2.4	-	2.5	-	Vdc	-	11	-	-	-	-	-	1	-	4	-	-	5,6,7,10
		12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	14	-	4	-	-	1,2,3,5,6, 7,10
Leakage Current	IOLK	11	-	1250	-	1250	-	1250	-	1250		1250	-	1250	μAdc	-	-	-	-	-	-	-	-	11	4	-	-	1,2,3,5,6, 7,10
		12		250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	١.	-	12	4	_	_	10,13,14
Short-Circuit Current	I _{SC}	11	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,10,11
		12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10,12,13,14
Output Voltage	v _{oh}	11	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	11	-	1	-	-	-	-	-	4	-	-	5,6,7,10
		12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	12	-	14	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,10
	v_{OL}	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	1	-	-	-	-	4	-		5,6,7,10
		12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0. 45	Vdc	12	-	-	-	14	-	-	-	-	4	-	-	1,2,3,5,6,

ELECTRICAL CHARACTERISTICS (continued)

							TE	ST CO	NDITIO	NS					
				mA							Volts				
(0)	② Test	ار	DL	Ic	Н		VIL	٧ _{IH}	V _R	V _{th 1}	V _{th O}	Vout	۷ _{cc}	V _{cch}	V _{IHX}
Tem	perature	Pr*	Std	Pr*	Std	lin	V IL	V IH	*R	Tth 1	*th O	out	*cc	, CCH	TIHX
(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	8.0	-
MC503*, MC553 {	+25°C	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
(+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5. 0	8.0	-
((0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4. 5	1.9	1.1	5.5	5.0	7.0	-
MC403*, MC453	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
I	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	7.0	_

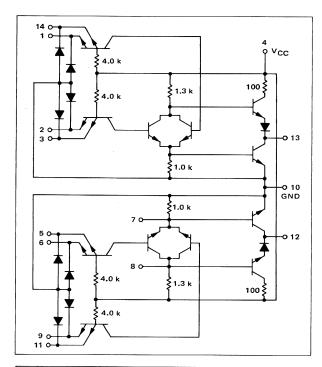
															1/3 C	20 10	-1. 2 -0. 0	2.0	0. 10	3.0	4. 0							4
		Pin		AC503						C403,							TEST CURI	RENT	/ VOLT	AGE A	PPLIED	TO P	INS LI	STED I	BELOW	/ :		
Characteristic	Symbol	Under Test	Min	5°C Max		25°C Max		25°C Max)°C Max		25°C Max		5°C Max	Unit	lor	Іон	l _{in}	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	V _{CCH}	V _{IHX}	Gnd
Power Requirements (Total Device)																												
Maximum Power Supply Current	I _{max}	4	-	34	-	34	-	34	-	24	-	24	-	24	m Adc	-	-	-	-	-	-	-	-	-	_	4	-	1,2,3,5,6, 7,10,13,14
Power Supply Drain	I _{PDH}	4	-	10	-	10	-	10	-	12	-	12	-	12	mAdc	-	-	-	-	-	-	-	-		4	<u> </u>	-	10
	I _{PDL}	4	-	10	-	10	-	10	-	12	-	12	-	12	mAdc	-		-	-	-	-	-	-	-	4	-	-	1,2,3,5,6 7,10
		4	-	7.0	-	7.0	-	7.0	-	7.0	-	7.0	-	7.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6 7,10,13,14
Switching Parameters										1						Pulse In	Pulse Out											
Turn-On Delay	ton 1	1, 11	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	11	-	-	-	-	-	-		4	-	2,3, 13,14	5,6,7,10
	t _{on 2}	11, 12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
Turn-Off Delay	t _{off 1}	1, 11	-	-	-	22	† -	-	-	-	Ħ	22	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
	t _{off 2}	11, 12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
Rise Time	t _{r 1}	1, 11	-	-	-	8.0	†-	-	-	-	-	8.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
	t _{r2}	11, 12	-	-	-	8.0	-	-	-	1-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
Fall Time	t _{f 1}	1, 11	† -	-	-	6.0	-	-	† -	-	-	6.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
	t _{f 2}	11, 12	-	-	-	5.0	-	-	-	† -	-	5.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10

^{*} Prime Fan-Out

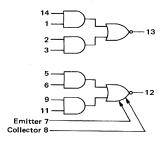
EXPANDABLE DUAL 2-WIDE 2-INPUT "AND-OR-INVERT" GATE

MTTL MC500/400 series

MC520 · MC570 MC420 · MC470



One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together and driving an output inverter with an output inverter with the ORing nodes made available for expansion. Up to 10 AND gates can be ORed together using the MC509 or MC510 expander series. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.

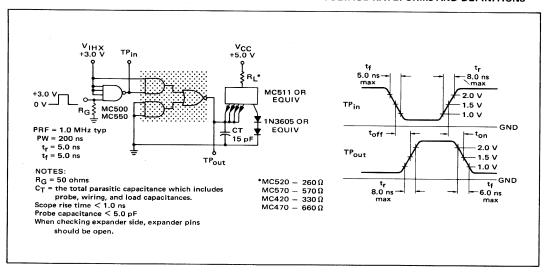


Positive Logic: $13 = \overline{(1 \cdot 14) + (2 \cdot 3)}$ $12 = \overline{(5 \cdot 6) + (9 \cdot 11) + (Expander)}$

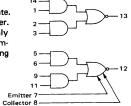
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(IF)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC520 MC570	1	(-1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC420 MC470	1	(-1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



							TE	ST CO	NDITIO	NS					
				mA							Volts				
(② Test	ار)L	Io	н	l _{in}	V _{IL}	V _{IH}	V _R	V _{th 1}	V,h 0	Vout	Vcc	V _{cch}	V _{IHX}
Ten	perature	Pr*	Std	Pr*	Std	'in	*IL	* ІН	* R	*th 1	* th O	out	• CC	· CCH	· IHX
1	_55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4. 5	2. 0	1.0	5.5	5.0	-	
MC520*, MC570	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4. 5	1.9	1.1	5.5	5.0	-	
MC420*, MC470	} +25℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4. 5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	<u> </u>

		Pin	N	IC520,	MC5	70 Tes				C420,				its	750		TEST CURR	ENT ,	VOLT	AGE A	PPLIED	TO P	INS LI	STED E	BELOW	/ :		
		Under	-5	5°C	+2	5°C		25°C		°C		5°C	+7		l l	1	,	$\overline{}$	V	V _{IH}	V _R	V _{th 1}	v	Vout	V _{cc}	V _{cch}	V _{IHX}	Gnd†
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	OL	Іон	lin	٧ _{IL}	Y IH	Y R	7 th 1	*th0	out	, cc	• ссн	· IHX	Gild1
Input Forward Current	I _F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	14		-	-	4	-	-	1,2,3,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	_	_	4	-		2,3,10,14
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10
Breakdown Voltage	BV _{in ''0''}	1	5. 5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	<u> </u>	-	4			2,3,10
	BV _{in "1"}	1	5. 5	-	5. 5		5. 5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-			_	-	4	_	_	2,3,10,14
Output	V	13	 	0.45	_	0.45	<u> </u>	0, 45	_	0, 45	_	0.45	-	0.45	Vdc	13	-	-	-	-	-	1	-	-	4	-	-	2,3,10
Output Voltage	V _{out ''0''} V _{out ''1''}	13	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	13	-	-	-	-	-	1	-	4	-	-	2,3,10
Leakage Current	I _{OLK}	13	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	† -	13	4	-	-	1,2,3,10,14
Homingo ourion	OLK								L .	<u> </u>			<u> </u>	<u> </u>	L.,			_	-	 		├	+-	+-	4		-	1,2,3,10,
Short-Circuit Current	I _{SC}	13	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-							13,14
Output Voltage	v	13	 -	0.40	+-	0,40	-	0.45	+-	0.40	-	0.40	-	0.45	Vdc	13	-	-	-	1	-	-	-	-	4	-	-	2,3,10
Output Voltage	V _{OL}	13	2.8		3.2	-	3.35	 -	3.0	-	3.1	-	3.15	-	Vdc		13	-	1	Ξ	-		Ē	Ē	4		<u> </u>	2,3,10
Power Requirements (Total Device) Maximum Power Supply Current	Imax	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	 - -	-	- 4	4	-	1,2,3,10,14
Power Supply Drain	I _{PDH}	4	-	14	-	14	-	14	-	18	-	18	-	18	mAdc	-		-	<u> </u>	<u> </u>	<u> </u>	-	+-	<u>-</u>	4	+-	<u>├-</u>	1,2,3,10,14
	I _{PDL}	4	-	7.0	-	7.0	-	7.0	-	8.0	-	8.0	-	8.0	mAdc	-	-	_		<u> </u>	LĪ.	Ĺ			Ļ	ļ	-	1,2,0,10,1
Switching Parameters									Π							Pulse In	Pulse Out		_	_		_	_	_	4	_	14	2,3,10
Turn-On Delay	ton	1,13	-	-	-	22	-	-	_	-	_	22	_	<u>_</u>	ns	1	13	Ľ	<u> </u>	<u> </u>		-	↓	1			7 -	1 1
Turn-Off Delay	t _{off}	1,13	-	1-	-	22	-	-	_	-	-	22	-	-	ns	1	13	Ŀ		<u> </u>	<u> </u>	<u> </u>	ļ-	ļ-	4	ļ- <u>-</u>	14	2,3,10
Rise Time	t _r	1,13	-	-	-	8.0	-	-	-	-	-	8.0	<u> </u>	-	ns	1	13	_	-			Ļ	<u> </u>	<u> </u>	4	ļ <u>-</u>	14	2,3,10
Fall Time	t _f	1,13	-	-	-	6.0	T-	Τ-	-	-	-	6.0	-	-	ns	1	13		-		-				4		14	2,3,10

^{*} Prime Fan-Out

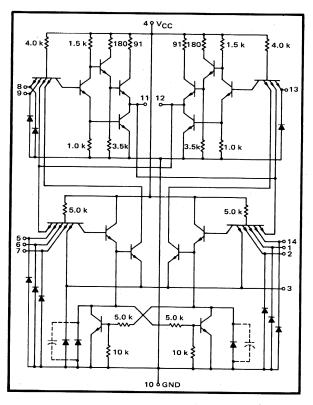
[†] Ground inputs to gates not under test during ALL tests unless otherwise noted.

[†] The inputs to all gates must be ungrounded.

MTTL MC500/400 series

"AND" J-K FLIP-FLOP

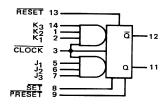
MC515 · MC565 MC415 · MC465



The MC415, MC465, MC515, and MC565 are clocked flip-flops that trigger on the negative edge and perform the JK logic function. Each flip-flop has an AND input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gating in counters and certain other applications. A direct SET, PRESET, and RESET are also available.

In normal operation, information is changed on the J and K inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is read into a temporary memory when the clock is in the high state. When the clock goes low, the information is transferred to the bistable section and the Ω and $\overline{\Omega}$ outputs respond accordingly. The information on the J and K inputs should not be changed while the clock is in the high state. Each flip-flop can be set or reset directly by applying the low state to the direct \overline{SET} , \overline{PRESET} , or \overline{RESET} inputs.

Since each flip-flop is a charge-storage device, there is a restriction on the clock fall time that must be observed.



	EQUIVALENT CIRCUIT	
SET 80- 90- PRESET	11 12	○13 RESET
J ₁ 5 0 J ₂ 6 0 J ₃ 7 0		014K3 01K2 02K1
V _{CC} = 4 GND = 10	ŢQXD.Ţ	CLOCK

J	K	a_n	a _{n+1}
0	0	0	0
0	0	1	1 1
0	1	0	0
0	1	1 .	0
1	0	0	1
- 1	0	1	1
1	1	0	1 1
1	1	1	0
1441			

Where $J = J_1 \cdot J_2 \cdot J_3$ $K = K_1 \cdot K_2 \cdot K_3$

Total Power Dissipation = 40 mW typ/pkg Switching Times:

t_{on} = 25 ns typ t_{off} = 13 ns typ

SERIES		OADING TOR	(1	F)			TEMPERATURE
02.11120	CLOCK	ALL OTHER	сьоск	ALL OTHER	OUTPUT DRIVE	(1 _O L)	RANGE
MC515 MC565	1.5	1	(-2.0 mA)	(-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates		-55°C to +125°C
MC415 MC465	1.5	1	(-2.5 mA)	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates		0°C to +75°C

MC515, MC565/MC415, MC465 (continued)

OPERATING CHARACTERISTICS

Clock fall time ≤ 150 ns.

Triggers on clock pulse widths ≥ 20ns.

Provides direct SET, PRESET, and RESET inputs. The application of a "0" state to 8 or 9, sets Q high; "0" state to 13, resets Q low. The clock must be in the low state when these functions are performed.

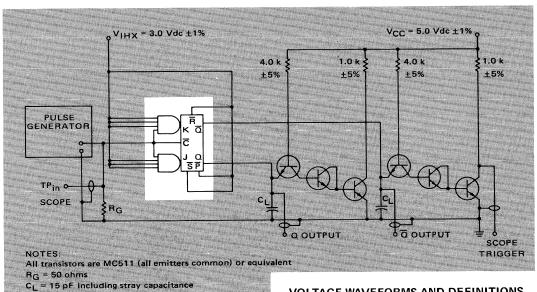
Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1"

state to "0" state information change on the J and K terminals. The flip-flop will require typically 10 ns to recognize a "0" state to "1" state change.

Negative edge triggering - When the clock goes from the high state to the low state, the information in the temporary storage section is transferred and the Q and $\overline{\mathbf{Q}}$ outputs will respond accordingly. While the clock is in a low state, the J and K terminals are inhibited.

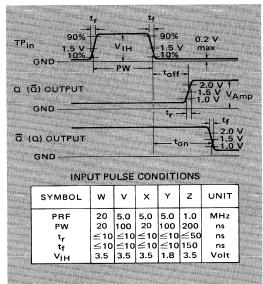
Unused J and K inputs should be tied to the clock or to 2.0 to 5.0 Vdc. PRESET and SET are tied to $\overline{\Omega}$; RESET is tied to Q.

FIGURE 1 – SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	toff	V	1000	20	ns
Delay Time On	ton	V	146	40	ns
Rise Time	tr	V	200	8.0	ns
Fall Time	tf	V	15.5-4	5.0	ns
Amplitude	VAmp	V	3.2	Selection of the select	Volt
(Device	WORST-C/ must toggle		The second second	pulse)	
TEST	SYMBOI	LIMI	TS	INP CONDI	
Toggle Frequence	y fTog	20 MH	z max	٧	V
Pulse Width	PW	20 ns r	nin	X	100 14 149
Input High Volt	age V _{IH}	1.8 V r	nin	Victoria Y	e news-est
Fall Time	The State of Land	150 ns	max	Z	Service of



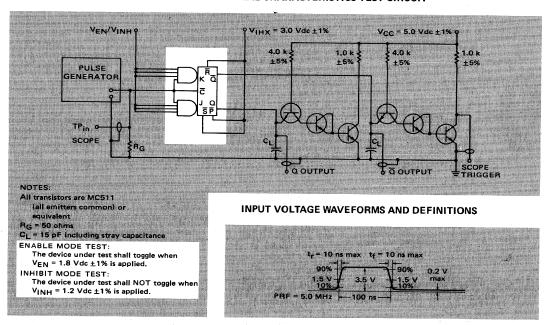
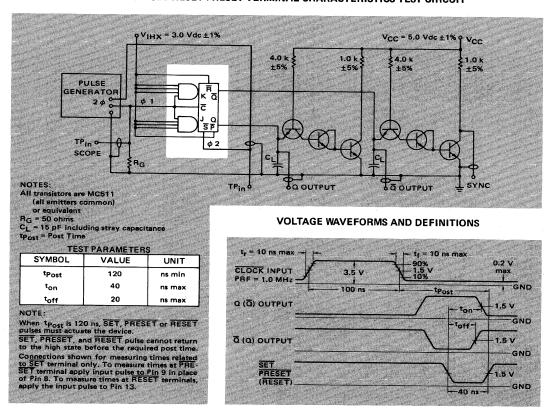
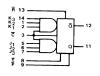


FIGURE 2 - J-K TERMINAL CHARACTERISTICS TEST CIRCUIT

FIGURE 3 - SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT



Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



								TES	T CON	IDITIONS									
				m/	1			Volts											
	@ Test	ار)L	I _c	I _{OH}		9 -	٠,	11	.,			1,,						
Te	Temperature			Pr*	Std	lin	2 l _{in}	VIL	V _{IH}	V _R	V _{th 0}	V _{th 1}	V _{out}	V_{cc}					
	(−55°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2. 0	5.5	5.0					
MC515*, MC565	{ +25℃	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.2	1.7	5.5	5.0					
	+125°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	0.9	1.4	5.5	5.0					
	(°°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.9	5.5	5.0					
MC415*, MC465	} +25℃	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0					
	(+75℃	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0					

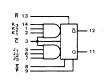
		Pin		AC515	MC	565 Te	ct lin	nite		MC415	MC	14E T	4 1 !		1		1 -1 -1 -1 -1	1	1 2.0	0. 10	1 0.0	4.0	11.1	1.1	13.3	3.0	
		Under		5°C		25°C		25°C	0			100 II		75°C	-		TEST CU	RRENT	r / voi	.TAGE	APPLI	ED TO PINS	LISTED	BELOW	۷:		
Characteristic	Symbol	Test						Max							Unit	lor	loh	l _{in}	2 I _{in}	VIL	V _{IH}	V _R	V _{th 0}	V _{th 1}	Vout	V _{cc}	Gnd
Input Forward Current	I _F	1	-	-1. 33				-1. 33		-1.66		-1.66		Ī	6 mAdo	-	-	-	-	-	-	2,3,5,6, 7,9,13,14	-	-	-	4	1,8,10
		5	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,6, 7,8,9,14	-	-	-		5,10,13
		8	-						- "		-		-					-		-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,13
		9	-		-		-				-		-			-		-	-	-	-	1,2,3,5, 6,7,8,14	-	-	-		9,10,13
		13	-	+	-	. +	_	•	-	•	-	+	-	+	ļ.,	-	-	-		-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,13
Leakage Current	I _R	1 5 8 9 13		100		100	-	100		100		100		100	μAdo	-	-			-	-	1 5 8 9	-	-	1111	4	2,3,5,6,7,10,11,14 1,2,3,6,7,10,12,14 1,2,3,5,6,7,9,10,12,14 1,2,3,5,6,7,8,10,12,14 1,2,3,5,6,7,10,11,14
Inverse Beta Current	IL	1 5 8 9 13		100	11111	100		100		100	-	100	-	100	μAde		-	-	-	8 13 ↓ ▼ 8		1 5 8 9	-	-	-	4	10
w Y and a	BV _{in"0"}	8 9 13	5.5	-	5.5	1 1 1 1	5.5		5.5		5.5	-	5.5		Vdc	- - - - -	-	1 5 8 9 13	-	8 13 ↓ 8	-	-	-	-		4	10
	BV _{in"1"}	1 5 8 9 13	5.5		5.5	-	5.5		5.5		5. 5		5.5		Vde	-		1 5 8 9 13	-		-	-		-	-	4	2,3,5,6,7,10,11,14 1,2,3,6,7,10,12,14 1,2,3,5,6,7,9,10,12,14 1,2,3,5,6,7,8,10,12,14 1,2,3,5,6,7,10,11,14

* Prime Fan-Out.

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



							TEST	r cond	ITIONS									
			mA				Volts											
Test	Io)L	I _{OH}			21	v	V	V	v	v	v	v					
erature	Pr*	Std	Pr*	Std	lin	Z Iin	A IF	VIH	¥R	V th O	th 1	V out	V _{cc}					
−55°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2.0	5.5	5.0					
+25°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4. 5	1.2	1.7	5.5	5.0					
+125°C │	20	10	-1.5	-0.7	1.0	2.0	0.45	2. 8	4. 5	0.9	1.4	5.5	5.0					
0°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4. 5	1.1	1.9	5.5	5.0					
+25°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0					
+75°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0					
	erature -55°C +25°C +125°C 0°C +25°C	erature Pr* -55°C 20 +25°C 20 +125°C 20 0°C 20 +25°C 20	erature	erature Pr* Std Pr* -55°C 20 10 -1.5 +25°C 20 10 -1.5 +125°C 20 10 -1.5 0°C 20 10 -1.2 +25°C 20 10 -1.2	erature Pr* Std Pr* Std -55°C 20 10 -1.5 -0.7 +25°C 20 10 -1.5 -0.7 +125°C 20 10 -1.5 -0.7 0°C 20 10 -1.2 -0.6 +25°C 20 10 -1.2 -0.6	erature Pr* Std Pr* Std	erature Pr* Std Pr* Std Inc. 2 Inc. -55°C 20 10 -1.5 -0.7 1.0 2.0 +25°C 20 10 -1.5 -0.7 1.0 2.0 +125°C 20 10 -1.5 -0.7 1.0 2.0 0°C 20 10 -1.2 -0.6 1.0 2.0 +25°C 20 10 -1.2 -0.6 1.0 2.0	erature Pr* Std Pr* Std In 2 I _{in} V _I -55°C 20 10 -1.5 -0.7 1.0 2.0 0.45 +25°C 20 10 -1.5 -0.7 1.0 2.0 0.45 +125°C 20 10 -1.5 -0.7 1.0 2.0 0.45 +25°C 20 10 -1.2 -0.6 1.0 2.0 0.45 +25°C 20 10 -1.2 -0.6 1.0 2.0 0.45	erature Pr* Std Pr* Std ln 2 ln VIL VIH -55°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 +25°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 +125°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 0°C 20 10 -1.2 -0.6 1.0 2.0 0.45 3.0 +25°C 20 10 -1.2 -0.6 1.0 2.0 0.45 3.0	erature Pr* Std Pr* Std I.o 2 I.o VI. VI. VR -55°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 4.5 +25°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 4.5 +125°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 4.5 0°C 20 10 -1.2 -0.6 1.0 2.0 0.45 3.0 4.5 +25°C 20 10 -1.2 -0.6 1.0 2.0 0.45 3.0 4.5	erature Pr* Std Pr* Std In 2 In VIL VIH VR V4ho -55°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 4.5 1.0 +25°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 4.5 1.2 +125°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 4.5 0.9 0°C 20 10 -1.2 -0.6 1.0 2.0 0.45 3.0 4.5 1.1 +25°C 20 10 -1.2 -0.6 1.0 2.0 0.45 3.0 4.5 1.1	erature Pr* Std Pr* Std ln 2 ln VIL VIH VR VthO Vth1 -55°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 4.5 1.0 2.0 +25°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 4.5 1.2 1.7 +125°C 20 10 -1.5 -0.7 1.0 2.0 0.45 2.8 4.5 0.9 1.4 0°C 20 10 -1.2 -0.6 1.0 2.0 0.45 2.8 4.5 0.9 1.4 +25°C 20 10 -1.2 -0.6 1.0 2.0 0.45 3.0 4.5 1.1 1.9 +25°C 20 10 -1.2 -0.6 1.0 2.0 0.45 3.0 4.5 1.2 1.8	erature Pr* Std Pr* Std lost lost Vin V					

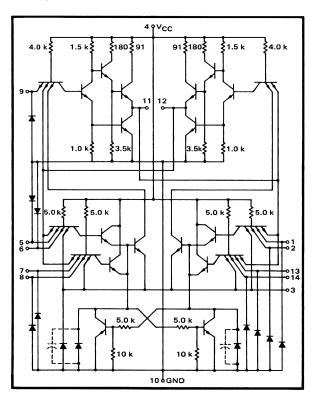
														' -	-/5 C	20 10	-1.2 -0.6	1.0	2.0	0.43	3.0	4.5	1.1	1. 7	3.3	3.0	
		Pin		MC515, MC565 Test Limits																							
Characteristic	Symbol	Under Test				Max			_	-			_		Unit	l _{OL}	l _{oн}	l _{in}	2 I _{in}	VIL	V _{IH}	V _R	V _{th 0}	V _{th 1}	V _{out}	V _{cc}	Gnd
Clock Input Forward Current	I _F	3	-	-2.0		-2.0		-2.0	-	-2.5	-	-2.5	-		mAdc	-	-	-	-	-	-	1,2,5,6, 7,8,9,13,14	-	-	-	4	3,10
Leakage Current	I _R	3	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-		-	-	3	-	-	-	4	1,2,5,6,7,10,14
Inverse Beta Current	I _L	3 3	-	150 150	-	150 150	-	150 150	-	150 150	-	150 150	-	150 150	μAdc μAdc	-	- '	-	-	13 8		3 3	-	-	-	4 4	10 10
	BV _{in''0''}		5.5 5.5	-	5.5 5.5	-	5.5 5.5		5.5 5.5	-	5. 5 5. 5	-	5. 5 5. 5	-	Vdc Vdc	-	-	-	3 3	13 8	:	-	-		=	4	10 10
	BV _{in"1"}	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5		Vdc	-		-	3	-		-	-		-	4	1,2,5,6,7,10,14
Output Output Voltage	v _{out ''0''}	12 11 11	-	0.45		0.45		0. 45	-	0.45	-	0.45	-	0.45	Vdc	12 11 11	- -	-	-	-	-	-	-	13 9 8	-	4	3,8,10 3,10,13 3,10,13
	v _{out "1"}	12 11 11	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2. 5	-	Vdc	- -	12 11 11	-	-	-	-		13 9 8	-	-	4 ↓	8,10 10,13 10,13
Leakage Current	IOLK	12 11	-	225 225	-	225 225	-	225 225	-	225 225	-	225 225	-	225 225	μAdc μAdc		-	-	-	-	-	-	-	-	12 11	4	1,2,3,5,6,7,8,9,10,13,14 1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	I _{SC}	12 11	-	-	-45 -45	-90 -90	-	-	-	-	-45 -45	-90 -90	-	-	mAdc mAdc	-	-	-	-	-	-	-	-		-	4	1,2,3,5,6,7,8,9,10,12,13,14 1,2,3,5,6,7,8,9,10,11,13,14
Output Voltage	V _{OL}	12 11 11	-	0.40	-	0.40	-	0. 45	-	0.40	-	0.40	-	0. 45	Vdc	12 11 11	-	-	-	-	13 9 8		-	-	- - -	4	3,8,10 3,10,13 3,10,13
	V _{ОН}	12 11 11	2.80	-	3. 20	-	3.35	-	3.00	-	3. 10	-	3. 15	-	Vdc	- - -	12 11 11	-	-	13 9 8	-		-	-		4 ↓	8,10 10,13 10,13
Power Requirements (Total Device) Power Supply Drain	I _{PD}	4 4	-	12 12	-	12	-	12 12	-	14 14	-	14	-		mAdc mAdc	-	-		-	-	- - -	-	-	-	-	4 4	3,10,13 3,8,10

^{*} Prime Fan-Out.

MTTL MC500/400 series

"OR" J-K FLIP-FLOP

MC516 · MC566 MC416 · MC466

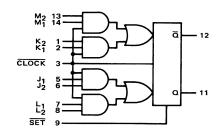


The MC516, MC566, MC416, and MC466 are clocked flip-flops that trigger on the negative edge and are internally wired to perform the J-K logic function. Each flip-flop has a positive logic AND-OR input gating configuration that consists of two clocked J inputs ANDed together, two clocked K inputs ANDed together, two clocked L inputs ANDed together, and two clocked M inputs ANDed together. The J and the L inputs are ORed together and the K and the M inputs are ORed together. A direct $\overline{\text{SET}}$ is also available.

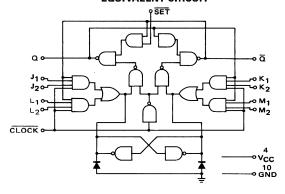
In normal operation, information is changed on the clocked inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory through the AND-OR input gating when the clock is in the high state. When the clock returns low the information in the temporary memory is transferred to the bistable section and the Q and the Q outputs respond accordingly. The information on the clocked inputs should not be changed while the clock is high.

Each flip-flop can be set directly by applying a low state to the direct SET input. Since each flip-flop is a charge storage device there is a restriction on the clock fall time that must be observed.

The AND-OR input configuration of each flip-flop makes it very useful for shift right/shift left registers and for up/down counters.



EQUIVALENT CIRCUIT



J	L	К	М	a _n	Q _{n+1}
0	0	х	×	0	0
1	X	×	×	0	1
×	1	х	х	0	1
×	x	0	0	1	1
×	х	1	x	1	0
×	x	х	1	1	0

X = Don't Care Where J = J₁ • J₂ L = L₁ • L₂ K = K₁ • K₂ M = M₁ • M₂

Total Power Dissipation = 60 mW typ/pkg Switching Times: ton = 25 ns typ toff = 13 ns typ

SERIES		OADING TOR	(1	lF)		OUTPUT DRIVE	(1)	TEMPERATURE
SEIMES	CLOCK	ALL OTHER	CLOCK	ALL OTHER		OUTFOI DRIVE	(IOL)	RANGE
MC516	3	4	(-4.0 mA)	(-1.33 mA)	15	MC500 series Gates	(20 mA)	5500
MC566	3	1	(-4.0 ma)	(-1.33 mA)	7	MC500 series Gates	(10 mA)	-55°C to +125°C
MC416	3	1	(50-4)	(1.55 - 1)	12	MC400 series Gates	(20 mA)	0°C to +75°C
MC466	3	'	(-5.0 mA)	(-1.66 mA)	6	MC400 series Gates	(10 mA)	000 10 +/500

MC516, MC566/MC416, MC466 (continued)

OPERATING CHARACTERISTICS

Clock fall time ≤ 150 ns.

Triggers on clock pulse widths ≥ 20 ns.

The application of a "0" state to the $\overline{\text{SET}}$ will cause Q to go to the "1" state. The clock must be in the low state when this function is performed.

Data at the clocked inputs must be present before the clock goes to a high state. If the information on the clocked inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1" state to "0" state change. The flip-flop will also require typically 10 ns to recognize a "0" state to "1" state change.

Negative edge triggering - When the clock goes from the high

state, the information in the temporary storage section is transferred; and the Ω and $\overline{\Omega}$ outputs will change accordingly. While the clock is in a low state, the J, K, L, and M terminals are inhibited.

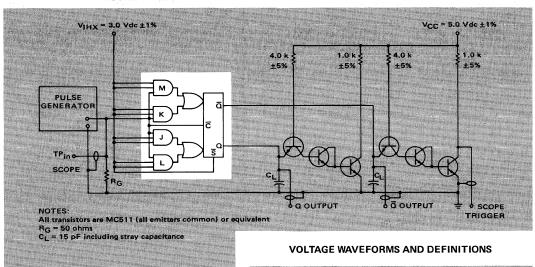
Unused Inputs:

Single unused J, K, L, and M inputs should be tied to the used input, to the clock input, or to 2.0 to 5.0 Vdc.

If both J, K, L, or M inputs are unused, they MUST be tied to ground.

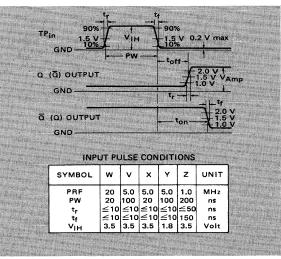
Unused \overline{SET} is tied to \overline{Q} .

FIGURE 1 - SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	toff	V		20	ns
Delay Time On	ton	V		40	ns
Rise Time		v		8.0	ns
Fall Time	tr	\$ V.		5.0	ns
Amplitude	VAmp	V	3.2	90,000	Volt
(Device	WORST-C must toggle		30 Table 1 Table 1	oulse)	
TEST	SYMBO	L LIMI	TS	INP CONDI	
Toggle Frequenc	y f _{Tog}	20 MH	z max	, v	i
Pulse Width	PW	20 ns	min	×	
Input High Volt	age VIH	1.8 V n	nin	Y	
Fall Time	t _f	150 ns	max	Z	



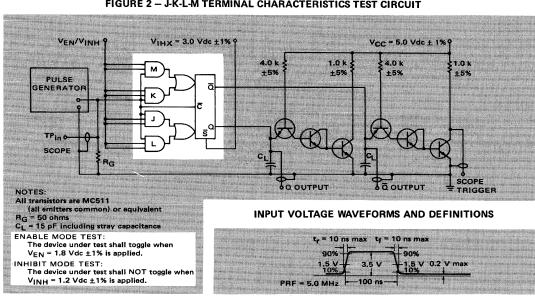
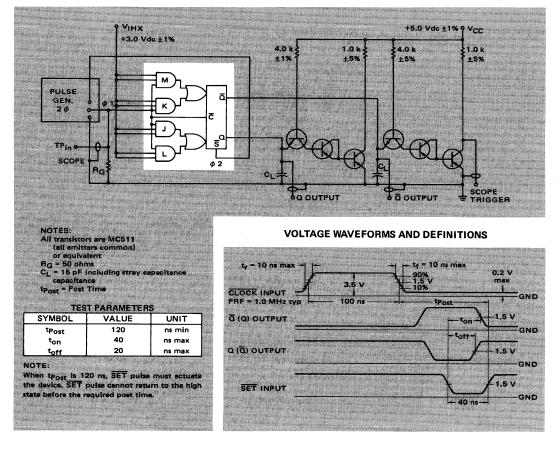


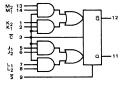
FIGURE 2 - J-K-L-M TERMINAL CHARACTERISTICS TEST CIRCUIT





ELECTRICAL CHARACTERISTICS Me 13=

Test procedures are shown for only one J, & 1/2 one K, and the SET input. The remaining J, K, L, M inputs are tested in the same manner.



								TEST	COND	ITION	5				
					mĀ							/olts			
	@ Test	Ic)L	ار	н				,,		v	.,	.,	v	v
Te	mperature	Pr*	Std	Pr*	Std	lin	2 I _{in}	4I _{in}	VIL	V _{IH}	V _R	V _{th 1}	V _{th O}	Vout	V _{cc}
	(−55°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
MC516*, MC566	₹ +25°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
•	(+125°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
	(0°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
MC416*, MC466	₹ +25°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.2	5. 5	5.0
	(+75°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

														(*/3 C	20 10	-1.2 -0.0				0		2.0					J.
	[·	Pin		MC516					_	MC416							TEST CUR	RENT	/ VOL	TAGE	APPLI	ED TO) PINS LIST	ED BEI	LQW:			
	1	Under	-5	5°C ∣	+2	5°C	+1:	25℃	0	τ	+2	5°C	+7	′5°C												14	114	1
Characteristic	Symbol	Test	Min	Max	Min	Max	Unit	lor	Іон	lin	2 l _{in}	4 I _{in}	VIL	VIH	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	Gnd								
Input Forward Current	I _F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	-	2,3,5,6,7, 8,13,14	-	-	-	4	1,9,10
		5	-		- 1		-		-		-		-			- -	- "	-	-	-	-	-	1,2,3,6,7, 8,13,14	-	-	-		5,10,11
		9	-		-		-		-		-		-			-	-	٠.		-	-	-	1,2,5,6,7, 8,13,14	-	-	-	•	3,9,10,11
Leakage Current	I _R	1 5 9	=	100	-	100	:	100	-	100	-	100	:	100	μAdc		-	-	-	-	-		1 5 9	-	-	=	4 ↓	2,3,5,6,7,8,10,11,13,14 1,2,3,6,7,8,9,10,12,13,14 1,2,3,5,6,7,8,10,12,13,14
Inverse Beta Current	IL	1 5 9	:	100	-	100	-	100		100	-	100	-	100	μAdc ↓	-	-	-	-	-	=	-	1 5 9	-	- -	-	4 ↓	9,10 10,11 10,11
Breakdown Voltage	BV _{in ''0''}	1 5 9	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	:	1 5 9	-	-	-	-	-	-	-	-	4	9,10 10,11 10,11
	BV _{in} "1"	1 5 9	5.5	-	5.5	=	5.5	-	5.5	-	5.5	-	5. 5	-	Vdc	=	=	1 5 9	-	-	-	:	-	-		-	4	2,3,5,6,7,8,10,11,13,14 1,2,3,6,7,8,9,10,12,13,14 1,2,3,5,6,7,8,10,12,13,14

^{*} Prime Fan-Out

① Momentarily ground pin prior to taking measurement at terminal.

ELECTRICAL CHARACTERISTICS (continued)

								TEST	COND	ITION	S				
					mΑ							Volts			
	@ Test	ار	DL .	١ _c	н								٠		
Ter	nperature	Pr*	Std	Pr*	Std	l _{in}	2 I _{in}	4 I _{in}	VIL	V _{IH}	V _R	V _{th} 1	V _{th o}	Vout	٧ _{cc}
	(−55°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
MC516*, MC566	{ +25℃	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
	(+125°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
	(0°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
MC416*, MC466	{ +25℃	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.2	5. 5	5. 0
	(+75°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

<u> </u>														· ·	T/3 C	20 10	-1.2 -0.0	1.0	2.0	4.0	0. 43	1 3.0	4.5 .	1.7	1.1	0.0	5.0	
		Pin Under			<u> </u>	66 Tes						66 Tes					TEST CUR	RENT	/ VOL	TAGE	APPL	IED T	O PINS LIST	TED BE	LOW:	-		
Characteristic	C			5℃		5°C		25°C	0			25°C		75°C												11/	V	
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Or	Іон	in	Z I _{in}	4I _{in}	VIL	VIH	V _R	V _{th 1}	Vtho	Vout	۷ _{cc}	Gnd
Clock Input Forward Current	I _F	3	-	-4.0	-	-4.0	-	-4.0	-	-5.0	-	-5.0	-	-5.0	mAdc	-	-	-	-	-	-	-	1,2,5,6,7, 8,13,14	-	-	-	4	3,10
Leakage Current	I _R	3	-	300	-	300	-	300	-	300	-	300	-	300	μAdc	-	-	-	-	-	-	-	3	-	-	-	4	1,2,5,6,7,8,10,13,14
Inverse Beta Current	I _L	3 3	-	400 400	-	400 400	-	400 400		400 400	-	400 400	-	400 400	mAdc mAdc	-	-	-	-	-	-	-	3 3	-	-	-	4 4	9,10 10,11
Breakdown Voltage	BV _{in ''0''}	3	5.5 5.5	-	5. 5 5. 5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	Vdc Vdc	-	-	-	-	3	-	-	-	-	-	-	4	10, 11 9,10
	вv _{in ''1''}	3	5.5	-	5. 5	-	5. 5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1 -	3	-	-	-	-	-	-	-	4	1,2,5,6,7,8,10,13,14
Output (For Set Only) Output Voltage	v _{out "0"}	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11①	-	-	-	-	-	-	-	9	-	-	4	3, 10
	v _{out "1"}	11	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	•	11	-	-	-	-	-	-	-	9	-	4	3,10
Leakage Current	IOLK	12 11	-	650 650	-	650 650	-	650 650	-	650 650	-	650 650	-	650 650	μAdc μAdc	:	:	-	-	-	-	-	12 11	-	:	:	4	1,2,3,5,6,7,8,10,11,13,14 1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	I _{SC}	12 11	-	-	-45 -45	-90 -90	-		1 1	-	-45 -45	-90 -90	-	-	mAdc mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,10,11,12,13,14 1,2,3,5,6,7,8,9,10,11,13,14
Output Voltage	v _{ОН}	12 11	2.80 2.80	-	3.20 3.20		3.35 3.35		3.00 3.00		3.10 3.10	-	3. 15 3. 15	-	Vdc Vdc	-	12 11	-	-	-	-	-	-	-	:	-	4	3,10,11 3,10,12
	V _{OL}	12 11	-	0.40 0.40	-	0.40 0.40	-	0. 45 0. 45		0. 40 0. 40	-	0. 40 0. 40	-	0.45 0.45	Vdc Vdc	12① 11①	-	-	-	-	:	9	-	-	:	-	4	3,10 3,10
Breakdown Voltage	OI	12 11	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	1, 1	4.25 4.25	-	4.25 4.25	-	4.25 4.25	mAdc mAdc	-	-	-	-	-	-	-	-	-	-	12 11	4	1,2,3,5,6,7,8,10,11,13,14 1,2,3,5,6,7,8,9,10,13,14
Power Requirements (Total Device)																												
Power Supply Drain	I _{PD}	4	-	12 12	-	12 12	-	12 12	-	14 14	-	14	-	14 14	Vdc Vdc	-	-	-	-	-	-	-	-	-	-	-	4	3,10,12
	1PD			12				- 12		14		14		14	vac	-	L		-	-	-	٠ ا		-	-	-	4	3,10,11

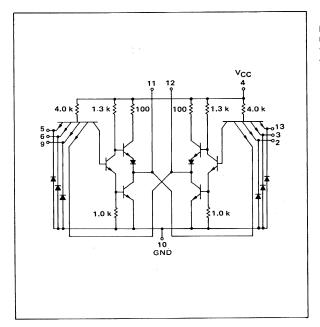
^{*} Prime Fan-Out

① Momentarily ground pin prior to taking measurement at terminal.

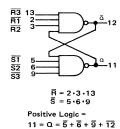
MTTL MC500/400 series

R-S FLIP-FLOP

MC513 · MC563 MC413 · MC463



This device consists of two independent dual 4-input NAND gates, internally cross coupled to realize a multiple input R-S flip-flop. The circuit can be used to eliminate switch contact bounce and to provide a temporary storage for data.



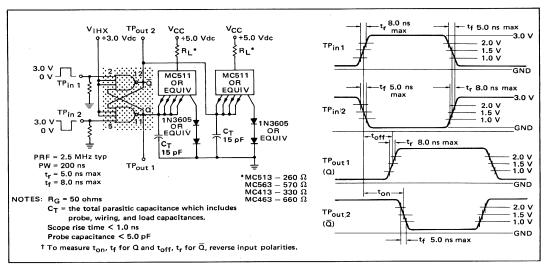
Total Power Dissipation = 30 mW typ/pkg Propagation Delay Time = 20 ns typ (to change state)

TRUTH TABLE (Positive Logic)

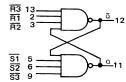
R	s	a	ā
0	0	Not Pe	rmitted
o	1	0	1
1	0	1	0
1	1	Q	₫

SERIES	INPUT LOADING FACTOR	(IF)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC513 MC563	1	(-1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC413 MC463	1	(-1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0°C to +75°C

SWITCHING TIME TEST CIRCUIT †



Test procedures are shown for only one input. The other inputs are tested in the same manner.



							TE	ST CO	NDITIO	NS			
				mA							Volts		
(@ Test	ار	DL .	Ic	Н		٧,,	V _{IH}	V _R	V _{th 1}	v	Vout	۷ _{cc}
Ten	nperature	Pr*	Std	Pr*	Std	lin	*11.	*IH	*R	Vth 1	V _{th 0}	out	*cc
1	_55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
MC513*, MC563	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
MC413*, MC463	} +25℃	20	10	-1. 2	-0.6	1.0	0.45	3.0	4.5	1.8	1. 2	5.5	5.0
	(+75℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

	ŀ	Pin		MC513	, MC	563 Te	est Lii	nits	٨	AC413	, MC4	163 Te	st Lin	nits		TEST	CURRENT /	VOLT/	AGE A	PPLIED	TO PII	NS LIS	TED BI	ELOW:		
		Under		55°C	+:	25°C	+1	25°C)°C		25°C		5°C			T .	Τ.						,		1.
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	Он	lin	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	Gnd
Input		Γ																	· · · ·			T				
Forward Current	I _F	2 5	-	-1. 33 -1. 33		-1. 33 -1. 33		-1. 33 -1. 33		-1.66 -1.66	-	-1.66 -1.66			mAdc mAdc	-	-	-	-	-	3,13 6,9	-	-	-	4	2,10 5,10
Leakage Current	I_R	2 5	-	100 100	-	100 100	-	100 100	-	100 100	-	100 100	-	100 100	μAdc μAdc	-	-	-	-	-	2 5	-		-	4	3,10,13 6,9,10
Inverse Beta Current	IL	2 5	-	100 100	-	100 100	-	100 100	-	100 100	-	100 100	-	100 100	μAdc μAdc	-	-	-	-	-	2 5	-	-	-	4	5,6,9,10 2,3,10,13
Breakdown Voltage	BV _{in"0"}	2 5	5. 5 5. 5	-	5.5 5.5	-	5. 5 5. 5	-	5.5 5.5	-	5. 5 5. 5	-	5. 5 5. 5	-	Vdc Vdc	-	-	2 5	-	-	-	-	-	-	4	5,6,9,10 2,3,10,13
	BV in "1"	2 5	5.5 5.5	-	5.5 5.5		5. 5 5. 5	-	5.5 5.5	-	5. 5 5. 5	-	5.5 5.5	-	Vdc Vdc	-	-	2 5	-	-	-	=	-	-	4	3,10,13 6,9,10
Output Output Voltage	V _{out "0"}	11	-	0.45	-	0.45	-	0.45	-	0. 45	-	0.45	-	0. 45	Vdc	11	-	-	-	-	-	5	-	-	4	2,3,10,13
	Vout "1"	11	2. 5	-	2.4	-	2.7	-	2.5	-	2. 4	-	2. 5	-	Vdc	-	11	-	-	-	-	-	5	-	4	2,3,10,13
Leakage Current	IOLK	11	- ,	1. 25	-	1. 25	-	1.25	-	1. 25	-	1. 25	-	1. 25	mAdc	-	-	-	-	-	-	-	-	11	4	5,6,9,10
Short-Circuit Current	ISC	11	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	5,6,9,10,11
Output Voltage	v _{OH}	11	2. 8	-	3. 2	-	3. 35	-	3.0	-	3.1	-	3. 15	-	Vdc	-	11	-	5	-	-	-	-	-	4	2,3,10,13
	V _{OL}	11	- 1	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	5	-	-	-	-	4	2,3,10,13
Power Requirements (Total Device)																										
Power Supply Crain	I _{PD}	4	-	-	-	9.0 9.0	-	-	-	-	-	9.0 9.0	-	-	mAdc mAdc	-	-	-	-		-	-	-	-	4	5,6,9,10 2,3,10,13
Switching Parameters																Pulse In	Pulse Out									
Turn-On Delay	t _{on} ‡	2, 12	-	- :	-	30	-	-	-	-	-	30	-	-	ns	2, 5	12	ļ -	-	-	-	-	-	-	4	10
Turn-Off Delay	t _{off} ‡	2, 11	-	-	-	20	-	-	-	-	-	20	-	-	ns	2, 5	11	-	-	-	-	-	-	-	4	10
Rise Time	t _r ‡	2, 11		-	-	8.0	-	-	-	-	-	8.0	-	-	ns	2,5	11	-	-	-	-	-	-	-	4	10
Fall Time	t, ‡	2, 12	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	2, 5	12	-	-	-	-	-	-	-	4	10

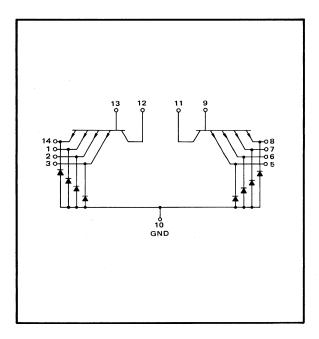
^{*} Prime Fan-Out

 $[\]mbox{\tt\it t}$ To measure $t_{on},\;t_{f}$ for Q and $t_{off},\;t_{r}$ for $\overline{Q},\;reverse$ input polarities.

DUAL 4-INPUT EXPANDER FOR "NAND" GATES

MTTL MC500/400 series

MC511 · MC561 MC411 · MC461



This device consists of two independent 4-emitter input transistors, each of which performs the positive logic AND function when used in conjunction with expandable gates. The base and collector of each device is available for expansion. Using the MC511 with the MC506 expandable gate, the number of AND inputs can be expanded to 20.



Total Power Dissipation = 0 mW typ/pkg Propagation Delay Time:

Δt_{pd} = +3.0 ns typ When added to the expandable "AND-OR-INVERT" gate.

 $\Delta t_{pd}/pF$ = +1.6 ns/pF typ Caused by additional capacitance at expander points.

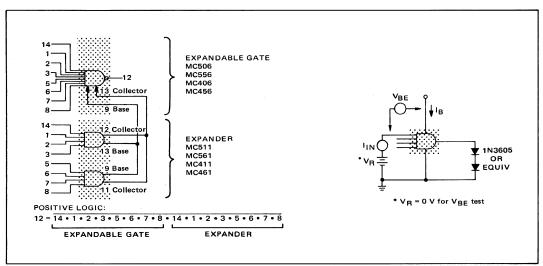
SERIES	INPU LOADI FACTO	NG (I _F)	TEMPERATURE RANGE
MC511 MC561	1	(-1.33 mA)	-55°C to +125°C
MC411 MC461	1	(-1.66 mA)	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

APPLICATION:

EXPANDABLE 8-INPUT "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED.

BVin "0", VBE, IL TEST CIRCUIT



Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



				TEST CO	NDITIONS		
,	@ Test		mA			Volts	
	nperature	l _{B1}	I _{B2}	l _{in}	V _R	V _{DC}	٧ _c
	(−55°C	1.33	1.0	1.0	4.5	**	1.5
MC511 , MC561	} +25°C	1.33	1.0	1.0	4.5	**	1.5
	(+125°C	1.33	1.0	1.0	4.5	**	1.5
	(0°C	1.66	1.0	1.0	4.5	**	1.5
MC411 , MC461	{ +25°C	1.66	1.0	1.0	4.5	**	1.5
	(+75°C	1.66	1.0	1.0	4.5	**	1.5

		Pin	A	AC511	MC	61 Te	ct lin	ite	٨	AC411.	MC	161 Te	stlim	its	1	TECT CUD	DENT (NO	TACE AD	DUITD TO	DINC LICTE	D DELOW	
		Under		5°C		25°C		25°C		°C	-	25°C		5°C	1	1EST COR	KENT / VO	LIAGE AP		T	D BELOW:	
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	l _{B1}	B2	lin	V _R	V _{DC}	۷ _c	Gnd†
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	13	-	-	1	-	-	2,3,10,14
Inverse Beta Current	$^{\mathrm{I}}\mathrm{_{L}}$	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	13	-	1	12	-	10
Breakdown Voltage	BV _{in ''0''}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	13	1	-	12	-	10
	BV _{in ''1''}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	13	-	1	-	-	-	2,3,10,14
Base-Emitter Voltage	V _{BE}	13, 1	-	1.3	-	1.1	-	1.0	-	1.3	-	1.2	-	1.1	Vdc	13	-	-	-	12	-	1,10
Base-Collector Voltage	V _{BC}	13, 12	-	1.3	-	1.1	-	1.0	-	1.3	-	1.2	-	1.1	Vdc	-	13	-	-	-	-	10,12
Offset Voltage	v _o	12*	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	Vdc	13	-	-	-	-	-	1,10
Forward Beta	$^{ m h}_{ m FE}$	12	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	-	13	-	-	-	-	12 ‡	1,10

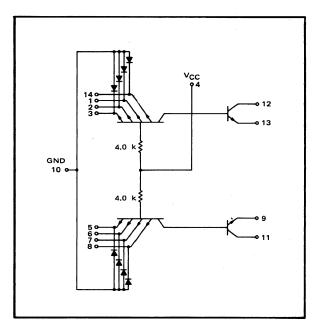
[†] Ground inputs to expanders not under tests during ALL tests

^{*} Measure V_O from Pin 12 to gnd ** Voltage obtained with two series diodes tied from collector to gnd. ‡ Measure I_C and calculate Beta. $\left(h_{FE} = \frac{I_C}{I_B}\right)$

DUAL 4-INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL MC500/400 series

MC510 · MC560 MC410 · MC460



This device consists of two independent 4-input AND gates. The outputs of each gate are made available as ORing nodes. Using the MC509 series and the MC510 series with any one of the basic expandable gates, up to 10 AND gates can be ORed together.



Total Power Dissipation = 10 mW typ/Pkg.

Propagation Delay Time:

 Δt_{pd} = +1.0 ns typ When added to the expandable "AND-OR-INVERT" gate.

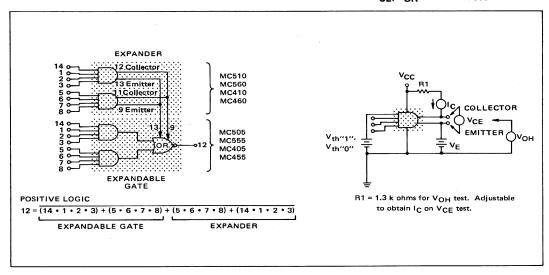
 $\Delta t_{pd}/pF = +1.0 \text{ ns/pF typ}$ Caused by additional capacitance at expansion points.

SERIES	INPUT LOADING (I _F) FACTOR	TEMPERATURE RANGE
MC510 MC560	1 (-1.33 mA)	-55°C to +125°C
MC410 MC460	1 (-1.66 mA)	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 2-WIDE 4-INPUT, "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EX-PANDER CONNECTED.

VCE, VOH TEST CIRCUIT



Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



							TEST	CON	DITION	IS				
(@ Test	m	A						Volt	s				
Ten	nperature	Ic	l _{in}	V _R	VEI	V _{E2}	V _{E3}	V _{th 1}	V _{th 0}	V _{out}	$V_{\rm CR}$	V _{CRH}	V _{cc}	V_{CCH}
	(−55°C	4.0	1.0	4.5	1.00	0.90	0.8	2.0	1.0	5.5	*	-	5.0	-
MC510 , MC560 -	+25°C	4.0	1.0	4.5	0.85	0.75	0.8	1.7	1.2	5.5	*	**	5.0	8.0
	(+125℃	4.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-
	(0°C	4.0	1.0	4.5	0.90	0.80	0.8	1.9	1.1	5.5	*	-	5.0	-
MC410 , MC460	} +25℃	4.0	1.0	4.5	0.85	0.75	0.8	1.8	1.2	5.5	*	**	5.0	7.0
	(+75℃	4.0	1.0	4.5	0.75	0.65	0.8	1.7	1.1	5.5	*		5.0	-

		Pin	М	C510,	MC5	50 Tes	t Limi	ts	N	IC410,		60 Te					Т	FST (I	IRRFN	T / VC	I TAGI	: APP	I IFD 1	O PIN	s list	ED BELO	ow:		
	l	Under	-5	55°C	+2	25°C	+13	25°C	()°C	+2	25°C	+7	′5°C	-	ļ				<u> </u>		r	т —					T	1 . 1
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Ic	l _{in}	V _R	VEI	V _{E2}	V _{E3}	V _{th 1}	V _{th O}	Vout	V _{CR}	V _{CRH}	Vcc	V _{CCH}	Gnd [†]
Input Forward Current	I_	1	_	-1.33	_	-1.33	_	-1.33	_	-1.66	_	-1.66	_	-1.66	mAdc	_	_	2,3,14	_	_	_	_	_	_	-		4	_	1,10
TOTWARA GALLONG	¹F								├	<u> </u>		 					-	-,-,-											
Leakage Current	$^{ m I}_{ m R}$	1	-	100	-	100	-	100	-	100	-	100	-	100	μ Adc			1	-	<u> </u>	-	-	-	-	-	-	4	-	2,3,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	_	100	-	100	μAdc	-	-	1	13	-	-	-	-	-	12	-	. 4	-	10
Breakdown Voltage	вv _{in''0''}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	13	-	-	-	-	-	12	-	4	-	10
	BV _{in"1"}	1	5.5		5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	<u> </u>	-	-	-	-	-	-	-	-	4	-	2,3,10,14
Output																													
Output Voltage	v _{он}	12	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	Vdc	-	-	-	-	13	-	-	1	-	12	-	4	-	10
	v _{CE} ①	12	-	0. 65	-	0.65	-	0.65	-	0. 65	-	0.65	-	0.65	Vdc	12	-	-	13	-	-	1	-	-	-	-	4	-	10
Leakage Current	IOLK	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	13	-	-	12	-	-	4	-	1,2,3,10,14
Power Requirements																													
(Total Device) Maximum Power Supply Current	I _{max} ②	4	-	-	-	10	-	-	-	-	-	10		-	m Adc	-	-	-	-	-	9,13	-	-	-	-	11, 12	-	4	1,2,3,10,14
Power Supply Drain	I _{PDH}	4	-	2.5	-	2.5	-	2.5	-	3.0	-	3.0	-	3.0	mAdc	-	-	-	-	-	9,13	-	-	-	-	-	4	-	10‡
	I _{PDL}	4	-	3.0	-	3.0	-	3.0	-	3.5	-	3.5	-	3.5	m Adc	-	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,10,14

^{*} Indicated pins tied to V_{CC} thru 1.3 k ohms ± 1.0% resistor. ** Indicated pins tied to V_{CCH} thru 1.3 k ohms ± 1.0% resistor.

[†] Ground inputs to gate not under test during ALL tests, unless otherwise noted.

[‡] The inputs of both gates must be ungrounded.

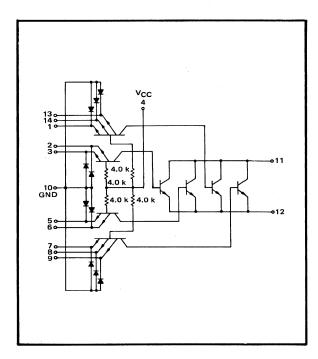
 $[\]textcircled{0}$ V_{CE} is referenced to the emitter voltage (Pin 13). The other gate is referenced to (Pin 9).

² Pin 9 ties to Pin 13. Pin 12 ties to Pin 11.

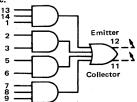
MTTL MC500/400 series

4-WIDE 3-2-2-3 INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MC509 · MC559 MC409 · MC459



This device consists of two 2-input and two 3-input AND gates ORed together with the common ORing nodes made available as the output. The basic expandable gate can be expanded up to 10 AND gates by using the MC509 series or the MC510 series expander package.



Total Power Dissipation = 20 mW/pkg.

Propagation Delay Time:

 $\Delta t_{pd} = \text{+4.0 ns typ (1.0 ns per ORed function)} \\ \text{When added to the expandable} \\ \text{"AND-OR-INVERT" gate.} \\$

 $\Delta t_{pd}/pF = 1.0$ ns/pF typ

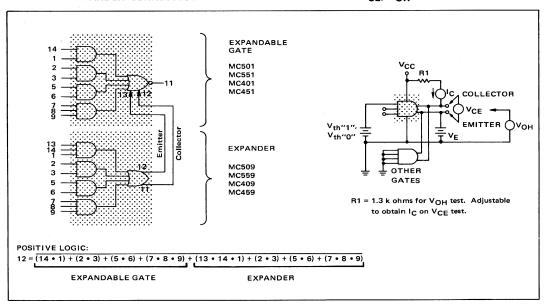
Caused by additional capacitance at expansion points.

SERIES	INPUT LOADING (I _F) FACTOR	TEMPERATURE RANGE
MC509 MC559	1 (-1.33 mA)	-55°C to +125°C
MC409 MC459	1 (-1.66 mA)	0°C to +75°C

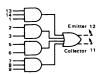
Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 4-WIDE "AND-OR-INVERT"
GATE WITH A 4-WIDE 3-2-2-3 INPUT EXPANDER CONNECTED.

VCE, VOH TEST CIRCUIT



Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



							T	EST C	DNDIT	IONS					
	(2 Test	m	Α						Volts					
		perature	l _c	l _{in}	V _R	VEI	V _{E2}	V _{E3}	V _{th 1}	V _{th O}	$V_{\rm out}$	$\mathbf{V}_{\mathbf{CR}}$	$V_{\rm CRH}$	V _{cc}	V_{CCH}
	(~-55°C	4.0	1.0	4.5	1.00	0.90	0.8	2.0	1.0	5.5	*	-	5.0	
MC509 , M	C559	+25°C	4.0	1.0	4.5	0.85	0.75	0.8	1.7	1.2	5.5	*	**	5.0	8.0
	1	+125°C	4.0	1.0	4. 5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-
		O°C	4.0	1.0	4.5	0.90	0.80	0.8	1.9	1.1	5.5	*	-	5.0	-
MC409 , M	C459	+25°C	4.0	1.0	4.5	0.85	0.75	0.8	1.8	1.2	5.5	*	**	5.0	7.0
		(+75°C	4.0	1.0	4.5	0.75	0.65	0.8	1.7	1.1	5.5	*	-	5.0	-

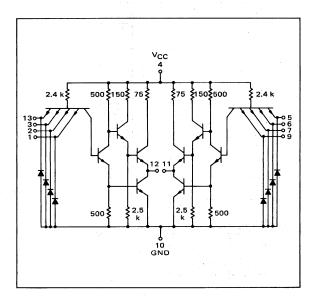
															. / 5 C	4.0	1.0	I	0. 10		0.0								
		Pin		MC509	, MC	559 Te	st Lin	nits	N	IC409,			st Lin	nits			T	EST CURR	ENT /	VOLT	AGE A	PPLIE	D TO F	PINS L	ISTED	BELOW	:		
		Under	5	55°C		25°C		25°C		°C		25°C		5°C		<u> </u>	_			17		W	W	V	1/	V	W	V	┥
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	l 'c	lin	V _R	VEI	V _{E2}	V _{E3}	V _{th 1}	V _{th O}	Vout	V _{CR}	V _{CRH}	٧ _{cc}	V _{ccн}	Gnd
Input Forward Current	I _F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	m Adc	-	-	2,3,5,6,7, 8,9,13,14		-	-	-	-	-	-	-	4	-	1,10
Leakage Current	$^{\mathrm{I}}\mathrm{_{R}}$	1	-	100	-	100	-	100	-	100	- "	100	-	100	μ A dc	-	-	1	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8, 9,10,13,14
Inverse Beta Current	I_{L}	1		100	-	100	-	100	-	100	-	100	-	100	μ A dc	-	-	1	12	-	-	-	_	-	11	-	4	-	2,3,5,6,7,8,9,10
Breakdown Voltage	BV in ''0''	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10
	BV _{in"1"}	1	5.5	-	5.5	-	5. 5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8,9, 10,13,14
Output																													
Output Voltage	V _{ОН}	11	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	Vdc	-	-	-	-	12	-	-	1	-	11	-	4	-	2,3,5,6,7,8,9,10
	v _{ce} ①	11	-	0.65	-	0.65	-	0.65		0.65		0.65	-	0.65	Vdc	11	-	-	12	-	-	1		<u> </u>	-	-	4	-	2,3,5,6,7,8,9,10
Leakage Current	I _{OLK}	11	-	250	-	250	-	250	-	250	-	250	-	250	μ A dc	-	-	-	-	-	12	-	-	11	-	-	4	-"	1,2,3,5,6,7,8, 9,10,13,14
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	20	-	-	-	-	-	20	-	-	mAdc	-	-	-	-	-	12	-	-	-	-	11	-	4	1,2,3,5,6,7,8, 9,10,13,14
Power Supply Drain	I _{PDH}	4 4	-	5.0	-	5. 0 6. 0	-	5. 0 6. 0	-	6.0	-	6.0	-	6.0	mAdc mAdc	-	-	-	-	-	12	-	-	-	-	-	4	-	10 1,2,3,5,6,7,8,
	1PDL	4	-	6.0	-	0.0	-	6.0	-	1.0	-	1.0	-	1.0	mAdc	_	-	-	-	-	-	-		_	_	-	*	-	9,10,13,14

^{*} Indicated pins tied to V_{CC} thru 1.3 k ohms \pm 1.0% resistor. ** Indicated pins tied to V_{CCH} thru 1.3 k ohms \pm 1.0% resistor. ① V_{CE} is referenced to the emitter Voltage (Pin 12).

MTTL MC500/400 series

DUAL 4-INPUT LINE DRIVER

MC507 · MC557 MC407 · MC457



Each of the two independent drivers in the package consists of a 4-input AND gate driving an output inverter. The output inverter is capable of supplying twice the drive of the basic gates. The line driver is especially useful for driving high capacitive loads or for driving large fan-outs such as the numerous clock inputs of large counters.



Positive Logic:
12 = 1 • 2 • 3 • 13

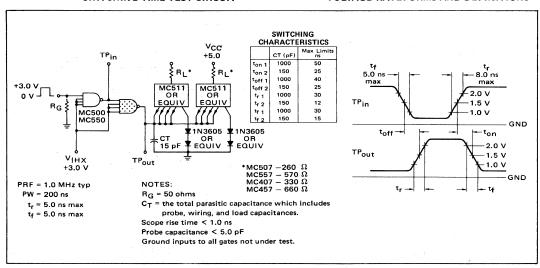
Negative Logic: 12 = 1 + 2 + 3 + 13

Total Power Dissipation = 60 mW typ/pkg Propagation Delay Time = 25 ns typ @ 1000 pF Load

SERIES	INPUT LOADING FACTOR (IF)	OUTPUT DRIVE (IOL)	TEMPERATURE RANGE
MC507 MC557	1.5 (+2.0 mA)*	30 MC500 series Gates (40 mA) 15 MC500 series Gates (20 mA)	-55°C to +125°C
MC407 MC457	1.5 (-2.5 mA)*	24 MC400 series Gates (40 mA) 12 MC400 series Gates (20 mA)	0°C to +75°C

^{*}Use I $_{\rm F}$ value of gate being driven (-1.33 or -1.66) to calculate output drive capability of line driver.

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one device. The other device is tested in the same manner. Further, test procedures are shown for only one input of the device under test. To complete testing, sequence through remaining inputs.



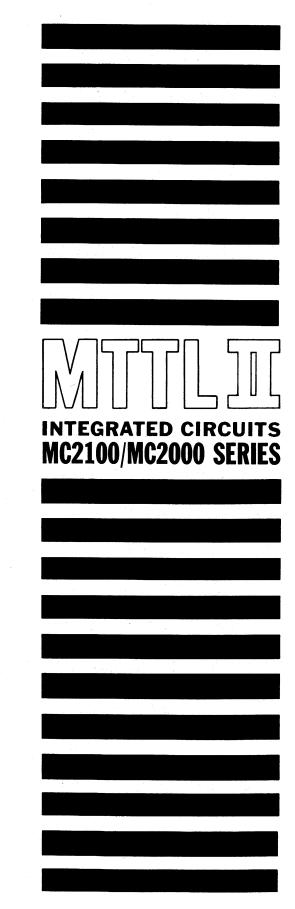
									TEST C	ONDITI	ONS						
				mΑ							Volts						
	@ Test	ار	DL .	Ic	ЭН		V _{IL}	V _{IH}	V _R	V _{th 1}	v	v .	V _{out 2}	۷٥١	V _{cc}	V _{ccH}	V _{IHX}
Te	mperature	Pr*	Std	Pr*	Std	'in	VIL.	* IH	*R	Tth 1	* th O	out 1	out 2	, or	*cc	*CCH	THX
	(-55°C	40	20	-3.0	-1.5	1.0	0.45	2.8	4.5	2.0	1.0	5.5	-	-	5.0	-	-
MC507*, MC557	} +25°C	40	20	-3.0	-1.5	1.0	0.45	2.8	4.5	1.7	1.2	5.5	6.5	8.0	5.0	8.0	3.0
	(+125°C	40	20	-3.0	-1.5	1.0	0.45	2.8	4.5	1.4	0.9	5.5	-	-	5.0	-	-
	(0°C	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.9	1.1	5. 5	-	-	5.0	-	-
MC407*, MC457	{ +25℃	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.8	1.2	5.5	6.5	8.0	5.0	7.0	3.0
	(+75°C	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.7	1.1	5. 5			5.0	-	-
MC457 Test Limits													CTED DE				

		Pin			'	57 Te						57 Te		nits		10 20			RRENT			APPLIE			ISTED B	ELOW	:	· · · · · · · · · · · · · · · · · · ·	L	
Characteristic	Symbol	Under Test		5°C Max		25°C Max		25°C Max		°C Max		25°C Max		75°C Max	Unit	l _{ot}	Гон	Iin	VIL	V _{IH}	V _R	V _{th 1}	V _{th 0}	V _{out 1}	V _{out 2}	۷ _{ol}	V _{cc}	V _{cch}	V _{IHX}	Gnd†
Input		_	_	_			_				\vdash			i –		<u> </u>	1	$\overline{\Box}$		Ħ		-				Ī				
Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	- 2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	2,3,13	-	-	-	-	-	4	-	-	1,10
Input Leakage Current	I_R	1	-	200	-	200	-	200	-	200	-	200	-	200	μAde	-	-	-	-	-	1	-	-	-	-	-	4	-	-	2,3,10,13
Inverse Beta Current	IL	1	-	200	-	200	-	200	-	200	-	200	-	200	μAde	-	-	-	-	-	1	-	-	-	-	-	4	-	-	10
Breakdown Voltage	BV _{in''0''}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	1	5.5	1	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	-	-	10
	BV _{in "1"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	_	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	<u> </u>	4	-	-	2,3,10,13
Output Output Voltage	V _{out ''0''}	12	-	0.45	-	0.45	-	0.45		0. 45	-	0.45		0.45	1	12	-	-	-	-	-	1	-	-	-	-	4	_	-	10
	V _{out "1"}	12	2. 5	-	2.4	-	2.7	-	2. 5	-	2. 4	Ι-	2. 5	-	Vdc	-	12	-	-	-	-	-	1	-	<u> </u>	-	4	-	-	10
Low Current MC507/407	I _{OL}	12	-	-	100	-	-	-	-	-	100	1	-	-	mAde		-	-	-	-	-	-	-	-	-	12	4 .	-	-	10
MC557/457		12	-	-	60	-	-	<u> </u>	-	-	60	-	-		m Ade		-	<u> -</u>	-	<u> </u>	<u> </u>	<u> </u>	-	-	-	12	4	<u> </u>	-	10
Breakdown Current	IO	12	-	-	-	1.0	-	-		-	-	1.0	<u> </u>	-	m Ade		-	-	-	_	-	-	<u> </u>		12		4	<u> </u>	-	1,2,3,10,13
Leakage Current	I _{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	_	-	12	-	-	4	-	-	1,2,3,10,13
Short-Circuit Current	I _{SC}	12	-50	-150	-50	-150	-50	-150	-50	-150	-50	-150	-50	-150	m Adc	-	-	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10,12,13
Output Voltage	v _{OH}	12	2.8	-	3. 2	-	3.35		3.0	-	3. 1	1	3.15	1	Vdc		12	-	1	-	-	-	-	-	-	-	4	<u> </u>	-	10
	VOL	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-		-			-	4	-	-	10
Power Requirements (Total Device)																														
Maximum Power Supply Current	I _{max}	4	-	-	-	15	-	-	-	-	-	15	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	4	-	1,5,10
Power Supply Drain	I _{PDH}	4	-	28	-	28	-	28		34	-	34	-	34	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	I _{PDL}	4	-	9	-	9	-	9	-	11	_	11	-	11	m Adc	-	-	-	-	-	-	-	-	-	-	-	4	-	-	1,5,10
Switching Parameters																Pulse In	Pulse Out													
Turn-On Delay	t _{on} ①	1,12	-	-	-	50 ①	-	-	-	-	-	50 Œ	1	-	ns	1	12	-	-	-	-	-		-	-	-	4	-	2,3,13	10
Turn-Off Delay	t _{off} ①	1,12	-	-	-	40 ①	-	-	-	-	_	40 ①	1	-	ns	1	12	-	-	-	-	_	-	_	_	-	4	-	2,3,13	10
Rise Time	t _r ①	1,12	-	-	-	30 ①	-	-	-	-	-	30 Œ	1	-	ns	1	12	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10
Fall Time	t _f ①	1,12	-	-	-	30 ①	-	-	-	-	-	30 Œ	-	-	ns	1	12	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10

^{*} Prime Fan-Out.

[†] Ground inputs to gates not under test during ALL tests, unless otherwise noted.
‡ The inputs to all gates must be ungrounded.

①Values @ 1000 pF load.



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AND J-K Flip-Flop

Dual 4-Input Expander for

AND-OR-INVERT Gates

AND-OR-INVERT Gates

4-Wide 3-2-2-3 Input Expander for

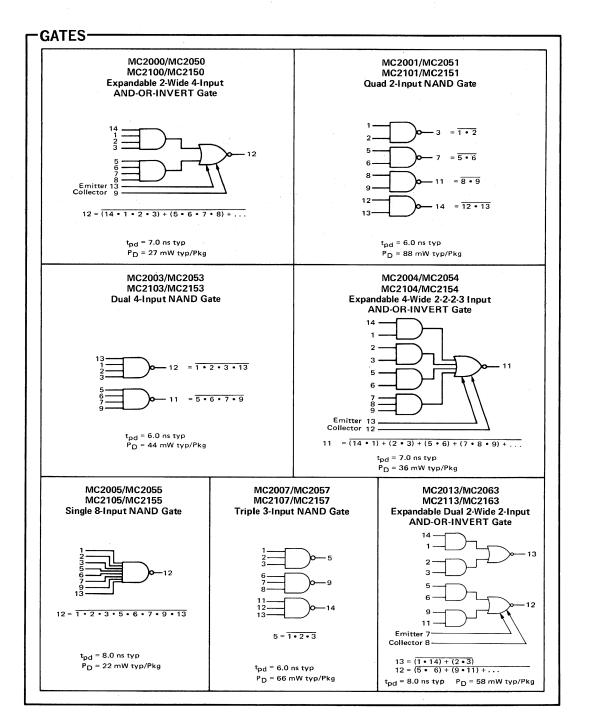
OR J-K Flip Flop

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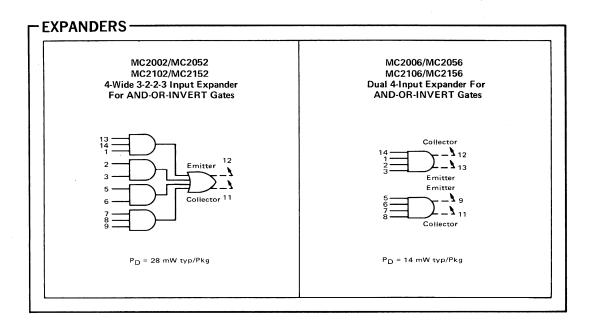
 $V_{CC} = 5.0 \text{ Vdc}, T_A = 25^{\circ} \text{C}$

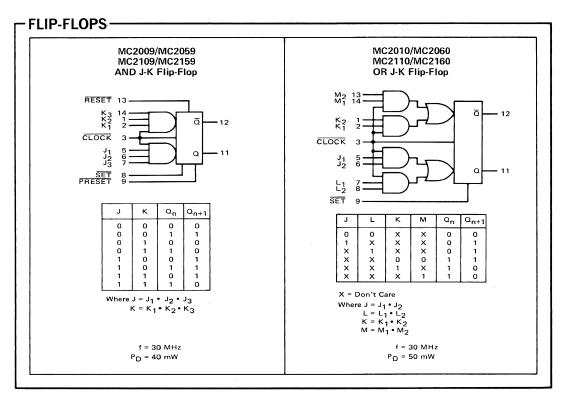
	T	ype	Out	put	Propagation		
Function	Case 609, 93	Case 609	Load Fac Each (- 1	Delay ^t pd	Power Dissipation mW	Page No.
	0 to +75 ⁰ C	-55 to +125 ⁰ C	MC2000 Series	MC2100 Series	ns typ	typ/pkg	
Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC2000 MC2050	MC2100 MC2150	9 5	11 6	7.0	27	4-66
Quad 2-Input NAND Gate	MC2001 MC2051	MC2101 MC2151	9 5	11 6	6.0	88	4-68
4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates	MC2002 MC2052	MC2102 MC2152	9 5	11 6	-	28	4-87
Dual 4-Input NAND Gate	MC2003 MC2053	MC2103 MC2153	9 5	11 6	6.0	44	4-64
Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate	MC2004 MC2054	MC2104 MC2154	9 5	11 6	7.0	36	4-70
Single 8-Input NAND Gate	MC2005 MC2055	MC2105 MC2155	9 5	11 6	8.0	22	4-62
Dual 4-Input Expander for AND-OR-INVERT Gates	MC2006 MC2056	MC2106 MC2156	9 5	11 6	· <u>-</u>	14	4-85
Triple 3-Input NAND Gate	MC2007 MC2057	MC2107 MC2157	9 5	11 6	6.0	66	4-72
AND J-K Flip-Flop	MC2009 MC2059	MC2109 MC2159	9 5	11 6	f = 30 MHz	40	4-76
OR J-K Flip-Flop	MC2010 MC2060	MC2110 MC2160	9 5	11 6	f = 30 MHz	50	4-81
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC2013 MC2063	MC2113 MC2163	9 5	11 6	8.0	58	4-74

LOGIC DIAGRAMS



LOGIC DIAGRAMS (continued)







GENERAL INFORMATION SECTION

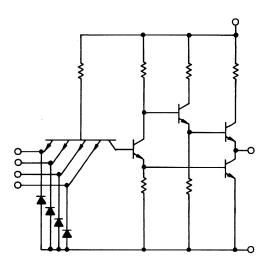
INTRODUCTION

MTTL II transistor-transistor logic is a high-speed, highnoise-immunity family of saturating integrated logic circuits.

The MTTL II family provides a speed extension of the medium-speed MTTL family. The circuits in the MTTL II family are identified by a multiple emitter input transistor and a two-stage active "pull-up" in the upper output network as shown in Figure 1.

The multiple emitter input configuration offers the maximum amount of logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The two-stage output configuration provides very low output impedances in each of the two output states. These low impedances result in excellent ac noise immunity and allow high-speed operation while driving large capacitive loads.

FIGURE 1 - TYPICAL MTTL II CIRCUIT



MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage — Continuous MC2100 Series MC2000 Series	+8.0 +7.0	Vdc
Supply Operating Voltage Range	4.5 to 6.0	Vdc
nput Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range MC2100 Series MC2000 Series	-55 to +125 0 to +75	°c
storage Temperature Range Flat Package Plastic Package	-65 to +200 -55 to +125	°c
Maximum Junction Temperature MC2100 Series MC2000 Series	+175 +150	°c
Thermal Resistance - Junction To Case ($ heta_{ m JC}$) Ceramic Flat Package Plastic Dual-In-Line	0.09 0.15	°C/mW
Thermal Resistance - Junction To Ambient (θ _{JA}) Ceramic Flat Package Plastic Dual-In-Line	0.26 0.30	°C/mW



GENERAL INFORMATION **SECTION**

TYPICAL CHARACTERISTICS

The following summary presents the typical operating characteristics of the MTTL II family. Unless otherwise indicated, the parameters are defined for V_{CC} = +5.0 volts and T_A = +25°C.

Supply Voltage Operating Range = 4.5 to 6.0 volts

Operating Temperature Range C2100/2150 Series = -55 to +125°C MC2000/2050 Series = 0 to +75°C

Output Drive Capability

Other Gates (Output Loading Factor):

MC2100 Series = 11 MC2100 or MC2150 Series Gates.

MC2150 Series = 6 MC2100 or MC2150 Series Gates.

MC2000 Series = 9 MC2000 or MC2050 Series Gates. MC2050 Series = 5 MC2000 or MC2050 Series Gates.

Capacitance = 600 pF

Output Impedance

High State = 10 ohms (unsaturated) nominal

Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits

+5.5 volts maximum

-0.5 volt minimum

Switching Threshold = 1.5 volts nominal

Input Impedance

High State = 400 k ohms nominal Low State = 2.5 k ohms nominal

Worst-Case DC Noise Margin

MC2100/2150 series 0.700 volt minimum High State -MC2000/2050 series 0.600 volt minimum

MC2100/2150 series 0.650 volt minimum Low State -

MC2000/2050 series

0.650 volt minimum

Power Dissipation 22 mW per gate typical 40-50 mW per flip-flop typical

Switching Speeds(1)

Average Propagation Delay = 6.0 ns per gate typical 15 ns per flip-flop typical

Rise Time = 1.0 ns typical Fall Time = 1.3 ns typical

Flip-Flop Clock Frequency (MC2109/MC2110 Series) = 30 MHz

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL, the designer must continually be aware of the fact that he is working with the fastest form of saturating logic available in the industry today. The switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions have been included to help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rate of change of currents and voltages for a single MTTL II gate is in the range of 107 A/s and 108 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL II circuits. A comparatively large, low-inductance type capacitor (in the 1.0 μF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 μF capacitors for every five packages throughout a breadboard is adequate to supress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The standard supply voltage of the MTTL II logic circuits is +5.0 Vdc.The typical average dc power dissipation is given for each MTTL II circuit. (2) It should be noted that the totem pole output common to all high level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.7 mW/MHz/output for a 15 pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL II circuits.

Unused Inputs and Unused Gates

The unused inputs of any MTTL II logic circuit should not be left open, and can either be tied to the used inputs or returned to the supply voltage. This will reduce any potential problems resulting from external noise. If the inputs are returned to the supply voltage, care should be taken to insure that the supply voltage does not exceed the maximum rated input voltage of 5.5 volts. If the supply can exceed 5.5 volts, the unused inputs must be returned to a lower voltage. The total number of inputs that can be tied to the output of any driving gate is 50. (This is defined as high state output loading factor.) It should be noted that the low state output loading rules must still be maintained. The minimum logical 1" level for the high state output loading is summarized for VCC = 5.0 V, V_{IL} = 0.45 V and I_{OH} = -5.0 mA:

MC2100/2150 Series - VOH = 2.7 volts minimum @ -55°C MC2000/2050 Series $-V_{OH} = 2.9$ volts minimum @ 0°C

The unused inputs of the various flip-flops may be tied back to their associated outputs. To determine which outputs are related to each set of inputs by internal feedback, refer to the circuit schematics.

The inputs of any unused gate in a package should be grounded. This places the gate in its lowest power condition and will help to eliminate unnecessary power drain.

Expanders and Expander Nodes

The ORing nodes of all the MTTL II AND-OR-INVERT gates are made available for expanding the number of AND gates to 10. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 0.7 ns/pF.

Output OR (AND) Function

Unlike the MDTL family of logic circuits, the outputs of the MTTL II logic circuits cannot be tied together to perform the output OR, or more correctly, the output AND function. If the outputs of the MTTL II family devices are tied together, it would be possible for the lower output transistor of one circuit and the upper output transistor of another circuit to be "on" simultaneously. This condition provides a low-impedance path from $V_{\hbox{\footnotesize{CC}}}$ to ground and the current that flows (approximately ISC) exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

Operating Characteristics of Flip-Flops

The general operating characteristics and restrictions for the MC2109/MC2110 series J-K flip-flops are as follows:

The clocked inputs are inhibited when the clock is in the low state, and data should be applied and allowed to settle. The clocked inputs are enabled when the clock goes high and data enters the flip-flop. The data is temporarily stored in the charge-storage section (temporary memory) while the clock is in the high state. This data is transferred to the bistable section on the negative clock transition.

The data on the clocked inputs should not be changed while the clock is in the high state. Data changes during this clock condition

require 300 ns settling time.

The direct SET, PRESET, and RESET inputs do not directly affect the charge-storage section and therefore should not be used while the clock is high. On the negative transition of the clock, previously stored data may override the asynchronous set output state. Further, the direct SET, PRESET, and RESET inputs do not



GENERAL INFORMATION SECTION

override the clock and will not control the state of the flip-flop until 100 ns after the negative transition of the clock. The clock signal must conform to the following boundary conditions at +125°C.

Maximum guaranteed clock frequency	= 30 MHz
Maximum clock fall time	= 100 ns
Minimum clock pulse width	= 15 ns
Minimum clock pulse amplitude	= 1.8 V
Maximum negative clock voltage	= -0.5 V

Note: These boundary conditions for operation are not defined as occuring simultaneously.

The transfer of data from the charge storage section to the bistable section is essentially an ac operation and thus results in the restriction of the clock fall time. If the clock fall time is greater than 100 ns, the information retained in the charge-storage section may not be transferred to the bistable section. The flip-flop will operate from very low frequencies to 30 MHz as long as the clock fall time is less than or equal to 100 ns.

Large negative clock excursions may cause incorrect data transfers to the bistable section during the transfer cycles. Therefore, the most negative clock signal should be limited to -0.5 volt.

(1) The switching characteristics of the MTTL II family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turnon delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2}$$
 ns.

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the nega tive transition of the output from the 2.0 V to the 1.0 V level.

$$P_{D} = \frac{|PDL + |PDH|}{2} (V_{CC})$$

where IpDL and IpDH are the typical dc current drains at V_{CC} =

MC2000/2050 and 2100/2150 MTTL II* series integrated circuits are electrically interchangeable with SUHL II1 series logic circuits as shown in the cross reference below.

SG SF		-55 to	+125 ⁰ C	0 to -	+75 ⁰ C
NUMBER	Description	Fan-Out = 11	Fan-Out = 6	Fan-Out = 9	Fan-Out = 5
SG210-213	Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC2100	MC2150	MC2000	MC2050
SG220-223	Quad 2-Input NAND Gate	MC2101	MC2151	MC2001	MC2051
SG230-233	4-Wide 3-2-2-3 Input Expander For AND-OR-INVERT Gates	MC2102	MC2152	MC2002	MC2052
SG240-243	Dual 4-Input NAND Gate	MC2103	MC2153	MC2003	MC2053
SG250-253	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate	MC2104	MC2154	MC2004	MC2054
SG260-263	Single 8-Input NAND Gate	MC2105	MC2155	MC2005	MC2055
SG270-273	Dual 4-Input Expander For AND-OR-INVERT Gates	MC2106	MC2156	MC2006	MC2056
-	Triple 3-Input NAND Gate	MC2107	MC2157	MC2007	MC2057
SF250-253	AND J-K Flip-Flop	MC2109	MC2159	MC2009	MC2059
SF260-263	OR J-K Flip-Flop	MC2110	MC2160	MC2010	MC2060
SG310-313	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC2113	MC2163	MC2013	MC2063

^{*}Trademark of Motorola Inc. †Trademark of Sylvania Electric Products, Inc.



GENERAL INFORMATION SECTION

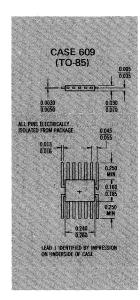
thost The minimal time necessary before the SET, PRESET, or RESET inputs can control the flip-flop after the negative clock edge DEFINITIONS tr Rise time Average increase in propagation delay per AND gate		SECTION	^t on	Turn-on delay time
BVin "0" Input breakdown voltage (ON level) BVin "1" Input breakdown voltage (OFF level) BVin "1" Input breakdown voltage (OFF level) Tog Toggle frequency C Collector current F Input forward current F Input forward current F Input forward current C F Corvard current of clock input F Input current F Input current C F Input current C F Input current C In Inverse beta current C Inway applied C Output breakdown current C Output breakdown current C Output breakdown current C Output leakage current C Output high voltage state C Output high voltage with log liowing into pin C Output high vol		SECTION	tPost	PRESET, or RESET inputs can control the flip-flop
BVin "1" Input breakdown voltage (OFF level) Trog Toggle frequency Collector current IFC Input forward current IFC Forward current of clock input Input current Input cur		DEFINITIONS	t _e	Rise time
Coplector current IF Input forward current IF Input forward current IFC Forward current of clock input Input current Inpu			Δt _{pd}	Average increase in propagation delay per AND gate of expander when connected to an AND-OR-INVERT gate.
Input forward current	10.00	医化氯化医抗医抗抗 医化抗抗抗性	Δt _{pd} /pF	
FC Forward current of clock input TPout Test point at output of device under test	50 S 00 S 90 S		TPin	Test point at input of device under test
In Input current VAmp Voltage amplitude	CE CONTRACTOR STATE		TPout	Test point at output of device under test
21 in 2-times the Input Current VCC Power supply voltage 41 in 4-times the Input Current VCCH High power supply voltage IL Inverse beta current VCE Collector-emitter voltage ILC Inverse beta current of the clock input VCR Collector voltage obtained thru 1.3 k ohm resistor from VCC. Imax Maximum rated power supply current with VCRH Collector voltage obtained thru 1.3 k ohm resistor from VCCH. IO Output breakdown current VE1, VE2, Emitter voltage IOL Output low current VE3, Enable voltage level IOLK Output leakage current VIH Voltage for high input voltage state IPDH Power supply drain with inputs low VIHX Reduced supply voltage to hold input above threshold and to prevent noise from entering the device IR Input reverse current with VR applied VIH Voltage for low input voltage state IRC Reverse current obtained from device output when one or more inputs are low VOH Output high voltage with IOH flowing out of pin IRC Prime Fan-Out VOL Output low voltage with IOH flowing into pin IRC Pulse repetition frequency Vout "0" Output high voltage with Vth "1" applied IRC Pulse width Voltage width Vth "0" applied IRC Pulse width Vth "0" applied	335 0.00			Voltage amplitude
4 lin			Vcc	Power supply voltage
Inverse beta current			Vccн	High power supply voltage
ILC Inverse beta current of the clock input Imax Maximum rated power supply current with VGR Collector voltage obtained thru 1.3 k ohm resistor from VCC. IO Output breakdown current IOH Output high current VE1. VE2. IOL Output low current VEN Enable voltage level IOLK Output leakage current VIH Voltage for high input voltage state IPDH Power supply drain with inputs high VIHX Reduced supply voltage to hold input above threshold and to prevent noise from entering the device IR Input reverse current with VR applied VINH Inhibit voltage level ISC Short circuit current obtained from device output when one or more inputs are low VOL Output low voltage with IOH flowing out of pin PRF Pulse repetition frequency VOUL Output high voltage with Vth "1" applied Std Standard fan-out VR Input reverse voltage VI Output high voltage with Vth "0" applied	100		VCE	Collector-emitter voltage
Maximum rated power supply current with Vmax applied VCRH Collector voltage obtained thru 1.3 k ohm resistor from VCCH.	→ 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1		t VCR	
Output breakdown current	I _{max}		with VCRH	Collector voltage obtained thru 1.3 k ohm resistor
IOH Output high current IOL Output low current VEN Enable voltage level IOLK Output leakage current IPDH Power supply drain with inputs high IPDL Power supply drain with inputs low IPDL Power supply drain with inputs low IR Input reverse current with VR applied IRC Reverse current of clock input ISC Short circuit current obtained from device output when one or more inputs are low IPC Prime Fan-Out IPC Prime Fan-Out IPC Pulse repetition frequency IPC Pulse width IPC Pulse wi	lo	Output breakdown current	VE1. VE2.	
IOLK Output leakage current VIH Voltage for high input voltage state VIHX Reduced supply voltage to hold input above thres- hold and to prevent noise from entering the device VIHX Reduced supply voltage to hold input above thres- hold and to prevent noise from entering the device VIHX Reduced supply voltage to hold input above thres- hold and to prevent noise from entering the device VIHX Reduced supply voltage to hold input above thres- hold and to prevent noise from entering the device VIHX Reduced supply voltage state VIHX Reduced supply voltage state VIHX Voltage for high input voltage state VIHX Voltage for low input voltage state Inhibit voltage level Vmax Maximum rated power supply voltage (VCC) VOH Output high voltage with IOH flowing out of pin VOHY OUT OUT OUTPUT high voltage with Vth "1" applied VOHY "1" Output high voltage with Vth "0" applied VR Input reverse voltage VR Input reverse voltage VIHX VIHX Reduced supply voltage tate VIHX Reduced supply voltage to hold input above threshold voltage VIHX Reduced supply voltage to hold input above threshold voltage vite voltage in put voltage input voltage voltage voltage VIHX VIHX Reduced supply voltage for high input voltage state VIHX Voltage for high input voltage state VINH Inhibit voltage input voltage input voltage voltage input voltage voltage VOHY ON OUTPUT high voltage with Vth "1" applied VOHY "1" Output high voltage with Vth "0" applied VR Input reverse voltage VR Input leverse voltage VINH Inhibit voltage voltage input voltage voltage VINH Inhibit voltage voltage input voltage voltage VINH Inhibit voltage voltage input voltage voltage VOHY ON OUTPUT high voltage voltage input voltage voltage VINH Inhibit voltage voltage VINH Inhibit voltage voltage voltage VOHY ON OUTPUT high voltage voltage voltag	Тон	Output high current		Emitter voltage
IPDH Power supply drain with inputs high VIHX Reduced supply voltage to hold input above thres hold and to prevent noise from entering the device IPDL Power supply drain with inputs low VIL Voltage for low input voltage state IR Input reverse current with VR applied VIL Voltage for low input voltage state IRC Reverse current of clock input VINH Inhibit voltage level ISC Short circuit current obtained from device output when one or more inputs are low VoH Output high voltage with IOH flowing out of pin Pr Prime Fan-Out VOL Output low voltage with IOH flowing into pin PRF Pulse repetition frequency Vout "0" Output low voltage with Vth "1" applied PW Pulse width Vout "1" Output high voltage with Vth "0" applied Std Standard fan-out VR Input reverse voltage tf Fall time Vth "0" Input logic "0" threshold voltage	IOL	Output low current	V _{EN}	Enable voltage level
IPDL Power supply drain with inputs low hold and to prevent noise from entering the device IR Input reverse current with VR applied VIL Voltage for low input voltage state IRC Reverse current of clock input VINH Inhibit voltage level ISC Short circuit current obtained from device output when one or more inputs are low Vmax Maximum rated power supply voltage (VCC) Pr Prime Fan-Out VOL Output high voltage with IOH flowing out of pin PRF Pulse repetition frequency Vout "0" Output low voltage with Vth "1" applied PW Pulse width Vout "1" Output high voltage with Vth "0" applied Std Standard fan-out VR Input reverse voltage tf Fall time Vth "0" Input logic "0" threshold voltage	JOLK	Output leakage current	ViH	Voltage for high input voltage state
IR Input reverse current with V _R applied IR Input reverse current with V _R applied VIL Voltage for low input voltage state VINH Inhibit voltage level VINH Inhibit voltage level VINH Inhibit voltage level VINH Inhibit voltage level VINH Inhibit voltage state VINH Inhibit voltage level VINH Inhibit voltage with IOH flowing out of pin INHIBIT VOLTAGE with IOH flowing out of pin INHIBIT VOLTAGE with IOH flowing into pin INHIBIT VOLTAGE with VINHIBIT VOLTAGE with VINHIBIT VOLTAGE with VINHIBIT VI	IPDH		VIHX	
IR Input reverse current of clock input IRC Reverse current of clock input ISC Short circuit current obtained from device output when one or more inputs are low ISC Short circuit current obtained from device output when one or more inputs are low ISC Output high voltage with IOH flowing out of pin ISC Output low voltage with IOH flowing into pin ISC Output low voltage with IOH flowing into pin ISC Output low voltage with IOH flowing into pin ISC Output low voltage with Vth "1" output low voltage with Vth "1" applied IST Output high voltage with Vth "0" applied INDUIT reverse voltage	IPDL	医多类性现象性结果 医电影电影电影	V.,	
Short circuit current obtained from device output when one or more inputs are low Pr Prime Fan-Out PRF Pulse repetition frequency PW Pulse width Std Standard fan-out Val Vmax Vmax Maximum rated power supply voltage (VCC) VOH Output high voltage with IOH flowing out of pin VoL Output low voltage with IOH flowing into pin Vout "0" Output low voltage with Vth "1" applied Vout "1" Output high voltage with Vth "0" applied Input reverse voltage VR Input reverse voltage Input logic "0" threshold voltage	IR			
when one or more inputs are low VOH Output high voltage with IOH flowing out of pin Pr Prime Fan-Out VOL Output low voltage with IOH flowing into pin PRF Pulse repetition frequency Vout "0" Output low voltage with Vth "1" applied PW Pulse width Vout "1" Output high voltage with Vth "0" applied Std Standard fan-out VR Input reverse voltage tr Fall time Vth "0" Input logic "0" threshold voltage	IRC		V	
PRF Pulse repetition frequency Vout "0" Output low voltage with Vth "1" applied PW Pulse width Vout "1" Output high voltage with Vth "0" applied Std Standard fan-out VR Input reverse voltage tf Fall time Vth "0" Input logic "0" threshold voltage	Isc		evice output	
PW Pulse width Vout "1" Output high voltage with Vth "0" applied Std Standard fan-out VR Input reverse voltage tf Fall time Vth "0" Input logic "0" threshold voltage	Pr	Prime Fan-Out	VOL	Output low voltage with IOL flowing into pin
Std Standard fan-out VR Input reverse voltage t _f Fall time Vth "0" Input logic "0" threshold voltage	PRF	Pulse repetition frequency	Vout "0"	Output low voltage with Vth "1" applied
t _f Fall time V _{th} "0" Input logic "0" threshold voltage	PW	Pulse width	Vout "1"	Output high voltage with Vth "0" applied
	Std	Standard fan-out	VR	Input reverse voltage
	ti _f	Fall time	Vth "0"	Input logic "0" threshold voltage
	30 M A 40 M	Turn-off delay time	V _{th} "1"	Input logic "1" threshold voltage

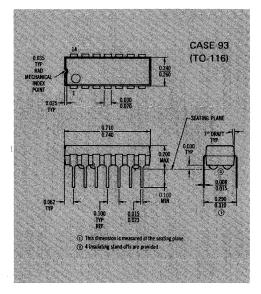
ton

Turn-on delay time

PACKAGING

All MTTL II integrated circuits are available in the TO-85, 14-lead flat package, MC2000 series is also available in the 14-lead dual in-line plastic package, To order the flat package, add suffix "F" to the basic type number; to order plastic package, add suffix "P".

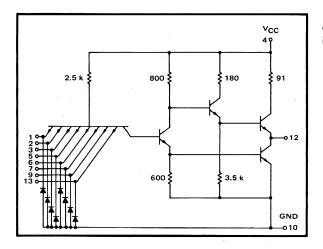




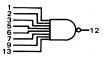
SINGLE 8-INPUT "NAND" GATE

MTTL II MC2100/2000 series

MC2105 · MC2155 MC2005 · MC2055



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders or decoders.

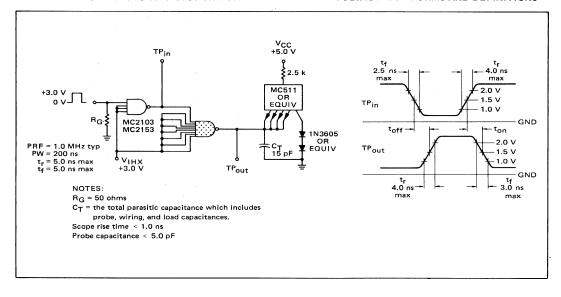


Positive Logic: 12 = 1 • 2 • 3 • 5 • 6 • 7 • 9 • 13 Negative Logic: 12 = 1 + 2 + 3 + 5 + 6 + 7 + 9 + 13

Total Power Dissipation = 22 mW typ/Pkg Propagation Delay Time = 8.0 ns typ

SERIES	INPUT LOADING FACTOR	(1F)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC2105 MC2155	1	-2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	-55°C to +125°C
MC2005 MC2055	1	–2.5 mA	9 5	MC2000 series Gates MC2000 series Gates		0°C to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



							TE	ST CO	NDITIO	NS					
				mΑ							Volts				
	@ Test	I _c	DL .	Ic	н		٧ _{IL}	٧ _H	V _R	V _{th 1}	V _{th 0}	V _{out}	۷ _{cc}	V _{CCH}	V _{IHX}
Ter	nperature	Pr*	Std	Pr*	Std	¹ in	11.	'IH	· R	'th I	* #h 0	out	,	CCH	IHA
4.	(−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	. 4. 5	2.0	0.9	5.5	5.0	-	-
MC2105*, MC2155	} +25℃	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	(+125°C	22.0	12.0	-2.2	-1.2	1.0	0,45	2. 7	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
MC2005*, MC2055	} +25℃	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	1 +75°C	22 5	12.5	-1 8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5. 5	5.0	-	-

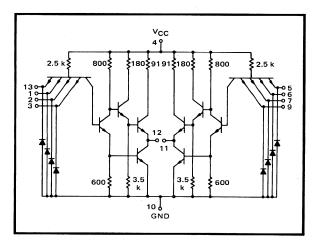
		Pin	M	C2105	MC2	2155 T	est Li	mits	MC	2005	. MC2	2055 1	est L			22.0 12.0	TEST CURR					TO P	INS II	STED	RFIOW			
		Under		55°C	<u>, </u>	25°C		25°C		°C		25°C		′5°C	1		TEST CORP	CENT .							,			
Characteristic	Symbol	Test						Max	Min	Max	Min	Max	Min	Max	Unit	lor	l _{он}	lin	VIL	V _{IH}	· V _R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	V _{cch}	V _{IHX}	Gnd
Input Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	m Adc	-	-		-	-	2,3,5,6 7,9,13	-	-	-	4	-	-	1,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	- '		-	-	İ	-	-	-	4	-	-	2,3,5,6,7, 9,10,13
Inverse Beta Current	I _{I.}	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	- 1	-	- 1	-	1	-	1 - 1	-	4		-	10
Breakdown Voltage	BV _{in''0''}	1	5. 5	-	5.5	-	5. 5	-	5.5	-	5.5	-	5, 5	-	Vdc	-	-	1 .	- '	- 1	-	-	1	- :	4	-	-	10
1	BV in "1"	1	5, 5	-	5.5	-	5, 5	-	5.5	-	5.5	-	5.5	-	Vdc	-	- :	1	- ;			-	-		4	- '		2,3,5,6,7, 9,10,13
Output Output Voltage	v _{out ''0''}	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	-	4	- '		10-
output totally	V _{out ''1''}	12	2.5	-	2.4	-	2.5		2.5	-	2.4		2.5	-	,V de	-	12	- ,	-	-	-	-	1	-	4	-		10-
Leakage Current	I _{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6,7, 9,10,13
Short-Circuit Current	I _{SC}	12	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	m Adc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7, 9,10,12,13
Output Voltage	V _{OL}	12 12	2. 70	0.40	3. 10	0.40	- 3. 15	0.45	- 2. 9	0.40	3.0	0.40	3.0	0. 45	V dc V dc	12	12	-	- 1	1 -	-	-	-	-	4	-	-	10 10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	6.50	-	-	-	-	-	6. 75	-	-	m Adc	-	-	-	-	-	-	-	-	-	-	4	-	1,10
Power Supply Drain	I _{PDH}	4 4	-	7.5	-	7.5 3.75	-	7. 5 3. 75	-	10 5.0	-	10 5.0	-	10 5.0	mAdc mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10 1,10
Switching Parameters	PDL				 		\vdash	-	┢			 	-	+	\vdash	Pulse In	Pulse Out			†				1				
Turn-On Delay	t _{on}	1,12	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Turn-Off Delay	toff	1,12	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Rise Time	t _r	1,12	-	-	-	4.0	-	-	-	-	-	4.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6 7,9,13	10
Fall Time	t _f	1,12	-	-	-	3.0	-	-	-	-	-	3.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10

^{*} Prime Fan-Out.

DUAL 4-INPUT "NAND" GATE

MTTL II MC2100/2000 series

MC2103 · MC2153 MC2003 · MC2053



This device consists of two 4-input NAND gates. The gates can be cross coupled to form a multiple-input R-S flip-flop or a circuit for eliminating contact bounce.

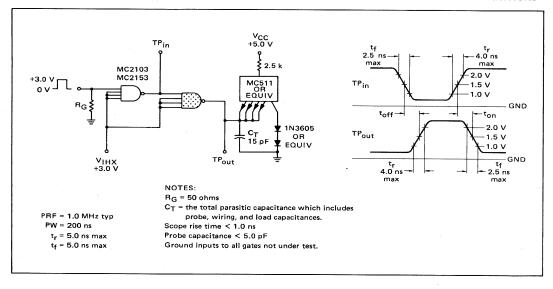


Positive Logic: $12 = \frac{1 \cdot 2 \cdot 3 \cdot 13}{1 \cdot 2 \cdot 3 \cdot 13}$ Negative Logic: $12 = \frac{1 \cdot 2 \cdot 3 \cdot 13}{1 \cdot 2 \cdot 3 \cdot 13}$

Total Power Dissipation = 44 mW typ/Pkg Propagation Delay Time = 6.0 ns typ

SERIES	INPUT LOADING FACTOR	(I _F)		OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC2103 MC2153	1	-2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	-55°C to +125°C
MC2003 MC2053	1	-2.5 mA	9 5	MC2000 series Gates MC2000 series Gates		0°C to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gate is tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. To complete testing, sequence through remaining inputs.



	. 1						TE	ST CO	NDITIO	NS					
				mΑ							Volts				
(@ Test	ار)L	Io	Н	1.	VIL	V _{IH}	V _R	V _{th 1}	V _{th 0}	ν.	۷ _{cc}	V _{CCH}	V _{IHX}
Ter	nperature	Pr*	Std	Pr*	Std	lin	· n	* IH	· R	*th I	· th U	OUT	- ((CCn	Inx
	(−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
MC2103*, MC2153	ໄ +25℃	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	(+125℃	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
MC2003*, MC2053	} +25℃	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
•	(+75℃	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

															-75													ř
		Pin		2103,								053 T					TEST CURR	ENT ,	/ VOLT	AGE A	PPLIED	TO P	NS LI	STED E	BELOW	:		ĺ
		Under	-5	5°C		5°C		25°C		°C		25°C	+7					ı.	٧,,	V _{IH}	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	V _{CCH}	VIHX	Gnd [†]
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lOr	I _{ОН}	in	'11	*IH	' R	* th I	* th U	out		ccn	IDA	Ond
Input Forward Current	I _E	1	-	-2.0	-	-2.0	-	-2.0	_	-2.5	-	-2.5.	-	-2.5	mAdc		-	-	-	-	2, 3, 13	-	-	· _	4	-	-	1,10
Leakage Current	I_{R}	1	-	100	-	100	-	100	-	100	-	100	-	100	μ A dc	-	-	-	-	-	1		-		4	-	<u> </u>	2, 3, 10, 13
Inverse Beta Current	I	1	-	100	-	100	-	100	-	100	-	100	-	100	μ Adc	-	-	-	-	-	1		-	-	4	-	<u> </u>	10
Breakdown Voltage	BV _{in"0"} BV _{in"1"}	1	5.5 5.5	-	5.5 5.5	-	5. 5 5. 5	-	5.5 5.5	-	5.5 5.5		5. 5 5. 5	-	V dc V dc	-	-	1	-	-	-	-	-	-	4	-	-	10 2, 3, 10, 13
Output Output Voltage	v _{out "0"} v _{out "1"}	12 12	- 2. 5	0. 45	- 2. 4	0. 45	2.5	0.45	- 2. 5	0.45	- 2. 4	0.45	- 2. 5	0.45	Vdc Vdc	12	12	-	-	-	-	1 -	1	-	4	-	-	10 10
Leakage Current	I _{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-		-	-	-	-	-	_	12	4	-	-	1, 2, 3, 10, 13
Short-Circuit Current	I _{SC}	12	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-		-	-	-	-	-	4		-	1, 2, 3, 10, 12, 13
Output Voltage	v _{OL}	12 12	- 2. 70	0.40	3. 10	0.40	3. 15	0. 45 -	2.9	0.40	3.0	0.40	3.0	0.45 -	V dc V dc	12 -	- 12	-	- 1	1 -	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	13	-	-	-	-	-	13.5	-	-	m Adc	-	-	-	-		-	-	-	-	-	4	-	1,5,10
Power Supply Drain	I _{PDH}	4	-	15 7. 5		15 7. 5	-	15 7.5	-	20 10	-	20 10	-	20 10	mAdc mAdc	-		-	-	-	-	-	-	-	4	-	-	10 [‡] 1,5,10
Switching Parameters			+-	-	 	 	1-	+	 	1-	\vdash			 		Pulse In	Pulse Out											
Turn-On Delay	t _{on}	1,12	-		-	10	-	-	-	-	-	10	-	-	ns	1	12	-	-		-		-	<u> </u>	4		2, 3, 13	
Turn-Off Delay	toff	1,12	1 -	-	-	10	-	t -	† -	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2, 3, 13	10
Rise Time	t _r	1,12	†-	-	-	4.0	-	-	-	-	-	4.0	T -	-	ns	1	12	-	-	-	-	<u> </u>		<u> -</u>	4	-	2, 3, 13	10
Fall Time	t.	1,12	-	1-	-	2.5	-	-	-	1 -	T-	2.5	-	-	ns	1	12	-	-	-	-		<u> </u>	<u> </u>	4		2, 3, 13	10

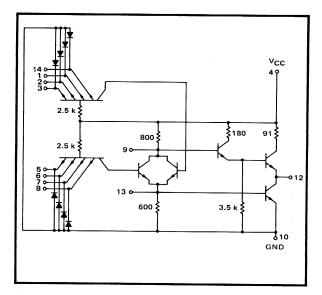
^{*} Prime Fan-Out.

[†] The inputs of both gates must be ungrounded.

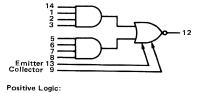
EXPANDABLE 2-WIDE 4-INPUT "AND-OR-INVERT" GATE

MTTL II MC2100/2000 series

MC2100 · MC2150 MC2000 · MC2050



This device consists of two 4-input AND gates ORed together and driving an output inverter. The ORing nodes are available for expansion, and up to 10 AND gates can be ORed together using the MC2102 or the MC2106 series expanders. Since switching speed is affected by the amount of capacitance on the expander nodes, care should be taken to minimize this capacitance to maintain switching speeds. This gate is usable for construction of half adders and other applications where the exclusive OR function is required.



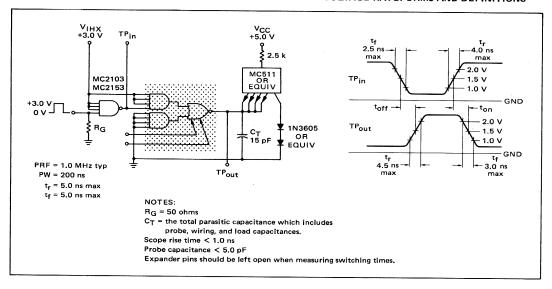
 $12 = (1 \cdot 2 \cdot 3 \cdot 14) + (5 \cdot 6 \cdot 7 \cdot 8) + (Expanders)$

Negative Logic: $12 = (1 + 2 + 3 + 14) \cdot (5 + 6 + 7 + 8) \cdot (Expanders)$

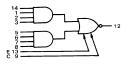
> Total Power Dissipation = 27 mW typ/Pkg Propagation Delay Time = 7.0 ns typ

SERIES	INPUT LOADING FACTOR	(IE)		OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC2100 MC2150	1	-2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	-55°C to +125°C
MC2000 MC2050	1 .	-2.5 mA	9 5	MC2000 series Gates MC2000 series Gates	22.5 mA 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



@ Test Temperatu						TE	ST CO	NDITIO	NS					
Temperatu			mΑ							Volts				
		OL	Ic	Н	_	VIL	V _{IH}	V _R	V _{th 1}	V _{th O}	v .	ν _{cc}	V _{CCH}	V _{IHX}
/	e Pr*	Std	Pr*	Std	lin	* 11.	'IH	· R	* th 1	* th O	out	- 66	· CCH	· IHX
(-55	C 22.0	12.0	-2. 2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
MC2100*, MC2150 🖁 +25	C 22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
(+125	C 22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
(0	C 22. 5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
MC2000*, MC2050 🚶 +25	C 22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
(+75	C 22. 5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	L <u>-</u>	-

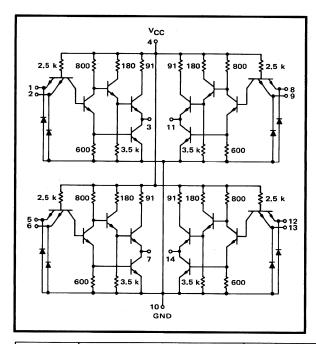
															.,,,	22. 0 12. 0	-1.0 -1.0	1.0	0. 10	1 2.0	1.0		1.0	10.0	1			1
		Pin	_	2100,						2000,							TEST CURF	RENT ,	/ VOLT	AGE /	APPLIED	TO P	INS L	ISTED	BELOW	/ :		
		Under		5°C		5°C		25°C		°C		25°C		5°C					V	V _{IH}	V _R	V	V _{th} (Vout	V _{cc}	V _{cch}	V _{IHX}	Gnd
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	l _{ОН}	l _{in}	٧ _{IL}	A IH	₹ R	V th 1	* th C	out	, cc	* CCH	TIHX	Gilu
nput Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	m Adc	-	-	-	-	-	2,3,14	-	-	-	4	-	-	1,5,6,7, 8,10
Leakage Current	IR	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	_	4	-	-	2,3,5,6,7, 8,10,14
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μ Adc	-	-	-	•	-	1	-	-	-	4	-	-	5, 6, 7, 8, 10
Breakdown Voltage	BV _{in"0"} BV _{in"1"}	1	5. 5 5. 5		5. 5 5. 5	-	5. 5 5. 5	-	5. 5 5. 5	l	5.5 5.5	-	5.5 5.5	-	Vdc Vdc	-	-	1	-	-	-	-	-	-	4	-	-	5, 6, 7, 8, 10 2, 3, 5, 6, 7, 8, 10, 14,
Output Output Voltage	v _{out ''0''} v _{out ''1''}	12	- 2. 5	0.45	2.4	0.45	- 2. 5	0.45	- 2.5	0.45	- 2.4	0. 45	- 2. 5	0.45	V dc V dc	12 -	12	-	-	-	-	1	- 1	-	4	-	-	5, 6, 7, 8, 10 5, 6, 7, 8, 10
Leakage Current	IOLK	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1, 2, 3, 5, 6, 7, 8, 10, 14
Short-Circuit Current	I _{SC}	12	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1, 2, 3, 5, 6, 7,8,10,12,1
Output Voltage	v _{OL}	12 12	2.70	0.40	- 3. 10	0.40	- 3. 15	0.45	2.9	0.40	3.0	0.40	3.0	0.45	V _e de V de	12 -	- 12	-	- 1	1 -	-	-	-	-	4	-	-	5, 6, 7, 8, 10 5, 6, 7, 8, 10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	10	-	-	-	-	-	11	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1, 2, 3, 5, 6, 7, 8, 10, 14
Power Supply Drain	I _{PDH}	4 4	-	9. 0 6. 0	-	9. 0 6. 0	-	9. 0 6. 0	-	12 7. 5	-	12 7. 5	-	12 7. 5	mAde mAde	1	-	-	-	-	-	-	-	-	4	-	-	10 1, 2, 3, 5, 6, 7, 8, 10, 14
Switching Parameters Turn-On Delay	ton	1,12	-	-	_	11	-	-	T -	-	-	11	-	_	ns	Pulse In	Pulse Out	-	-	-	-	-	-	-	4	-	2,3,14	5, 6, 7, 8, 10
Turn-Off Delay	toff	1,12		-	 -	11	-	 -	+-	-	† -	11	-	† -	ns	1	12	-	-	-	-	-	-	-	4	-	1	5, 6, 7, 8, 10
Rise Time	t	1,12		-	-	4.5	-	-	 -	-	-	4.5	-	T -	ns	1	12	-	1 -	-	-				4	-		5, 6, 7, 8, 10
Fall Time	t _e	1,12	T -	† -	-	3.0	1 -	-	T -	-	-	3.0	1 -	-	ns	1	12	-	-	-	-	T -		-	4	<u> </u>	2,3,14	5, 6, 7, 8, 10

^{*}Prime Fan-Out.

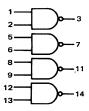
MTTL II MC2100/2000 series

QUAD 2-INPUT "NAND" GATE

MC2101 · MC2151 MC2001 · MC2051



This device consists of four 2-input NAND gates. The four gates in a single package represent increased functional flexibility. For example, a dual set-reset flip-flop may be obtained if each pair of gates is externally cross-coupled.

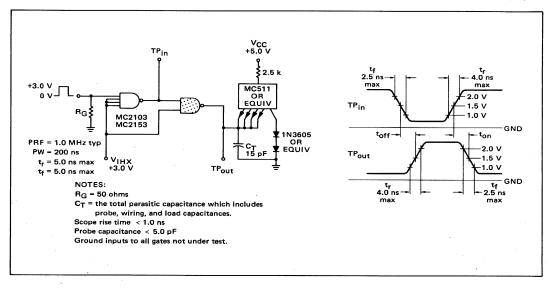


Positive Logic: $3 = 1 \cdot 2$ Negative Logic: 3 = 1 + 2

Total Power Dissipation = 88 mW typ/Pkg Propagation Delay Time = 6.0 ns typ

SERIES	INPUT LOADING FACTOR	(IF)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC2101 MC2151	1	-2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	-55°C to +125°C
MC2001 MC2051	1	-2.5 mA	9 5	MC2000 series Gates MC2000 series Gates	22.5 mA 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. The other input is tested in the same manner.



							TE	ST CO	NDITIO	NS					
				mA							Volts				
(@ Test	ار)L	J	Н		٧	v	v	v	V	٧	V	v	V _{IHX}
Ten	nperature	Pr*	Std	Pr*	Std	lin	٧	V _{IH}	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	V _{CCH}	*IHX
	_55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2. 0	0.9	5.5	5.0	•	-
MC2101*, MC2151	+25℃	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
MC2101 , MC2131	+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2. 9	4.5	1.9	1.0	5.5	5.0	-	-
AC2001*, MC2051	{ +25℃		12.5	-1.8	-1.0	1.0	0.45	2. 9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	(+75℃	22. 5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

																22.0			0. 10				1	0.0				
,		Pin			<u> </u>	2151 1				C2001							TEST CURI	RENT	/ VOLT	AGE A	PPLIED	TO P	INS LI	STED	BELOW	١.		
Characteristic	Symbol	Under Test		55°C Max		25°C Max		25°C Max		°C Max		25°C Max		5°C Max	Unit	lou	Гон	l _{in}	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	V _{ccH}	V _{IHX}	Gnd †
Input		-	1	1111111		1	1	1	1	1	1	111107		T T		1		 "				 		1				
Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAde	-	-	-	-	-	2	-	_	-	4	-	-	1,10
Leakage Current	I_{R}	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	 -	4	-	-	2, 10
Inverse Beta Current		1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV in "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	† -	4	-	-	10
	BV _{in"1"}	1	5.5	-	5.5	-	5, 5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,10
Output													 	 				 										
Output Voltage	v _{out ''0''}	3	-	0.45	-	0.45	-	0.45	-	0. 45	-	0. 45	-	0.45	Vdc	3	-	-	-	-	-	1	-	-	4	-	-	10
	v _{out ''1''}	3	2.5	-	2.4	-	2. 5	-	2.5	-	2.4	-	2.5	-	Vdc	-	3	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	IOLK	3	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	- '	-	-	-	-	-	-	3	4	-	-	1, 2, 10
Short-Circuit Current	I _{SC}	3	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	m Adc	-	-	-	-	-	1	-	-	-	4	-	-	1, 2, 3, 10
Output Voltage	v _{OL}	3	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	3	-	-	-	1	-	-	-	-	4	-	-	10
	v _{OH}	3	2. 70	-	3. 10	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	3	-	1	-	-	-	-	-	4	-	-	10
Power Requirements																												
(Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	26	-	-	-	-	-	27	-	-	mAde	-	-	-	-	-	-	-	-	-	-	4	-	1,5,8, 10,12
Power Supply Drain	I _{PDH}	4	-	30	-	30	-	30	-	40	-	40	-	40	m Adc	-	-	-	-	-	-	-	-	T -	4	-	-	10‡
	I _{PDL}	4	-	15	-	15	-	15	-	20	-	20	-	20	m Adc	-	-	-	-	-	-	-	-	-	4	-		1,5,8, 10,12
Switching Parameters									_				_	-		Pulse In	Pulse Out					<u> </u>		-				10,12
Turn-On Delay	t _{on}	1,3	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Turn-Off Delay	toff	1,3		-	-	10	-	-	_	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Rise Time	t _r	1,3	-	-	-	4.0	-	-	-	-	-	4.0	-		ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Fall Time	t _f	1,3	-	-	-	2.5	-	-	-	-	-	2.5	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10

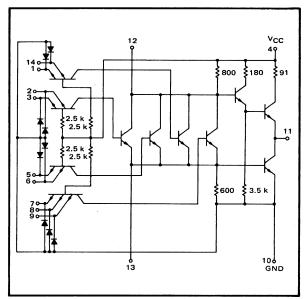
^{*}Prime Fan-Out

 $[\]uparrow$ Ground inputs to gates not under test during ALL tests unless otherwise noted. \ddag The inputs of all gates must be ungrounded.

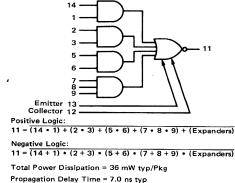
EXPANDABLE 4-WIDE 2-2-2-3 INPUT "AND-OR-INVERT" GATE

MTTL II MC2100/2000 series

MC2104 · MC2154 MC2004 · MC2054

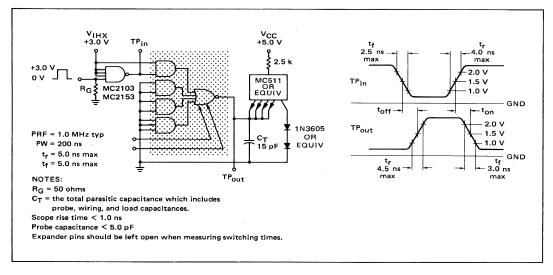


This device consists of three 2-input and one 3-input AND gates ORed together and driving an output inverter. The ORing nodes are made available for expansion, and up to 10 AND gates can be ORed together using the MC2102 or the MC2106 series expanders. Since switching speed is affected by the amount of capacitance on the expander nodes, care should be taken to minimize this capacitance to maintain switching speeds.

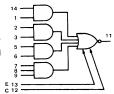


SERIES	INPUT LOADING FACTOR	(IF)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC2104 MC2154	1 -	-2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	-55°C to +125°C
MC2004 MC2054	1 -	-2.5 mA	9 5	MC2000 series Gates MC2000 series Gates	22.5 mA 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



 Te
MC2104*, MC2154
 MC2004*, MC2054

	2 1031
Ten	perature
((−55°C
, MC2154	+25°C +125°C
	+125°C

Test	ار	DL .	Io	Н	1
erature	Pr*	Std	Pr*	Std	Ľ
−55°C	22.0	12.0	-2.2	-1.2	1
+25°C	22.0	12.0	-2.2	-1.2	1.
⊦125°C	22.0	12.0	-2.2	-1.2	1
0°C	22.5	12.5	-1.8	-1.0	1
+25°C	22.5	12.5	-1.8	-1.0	1

						TE	ST CO	NDITIO	NS					
			mΑ							Volts				
it	l _c	OL .	Ic	Н	l _{in}	٧ _{IL}	V _{IH}	v	ν.	ν.	v	٧	V _{cch}	V _{IHX}
ure	Pr*	Std	Pr*	Std	'in	*1	*#	*R	*th 1	*th 0	* out	*cc	*CCH	'IHX
5°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2. 7	4.5	2.0	0.9	5.5	5.0	-	-
5°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
5°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
5°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
5°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

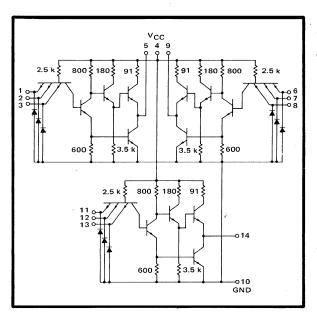
															+/5 C	22.5 12.5	-1.8 -1.0	1,0	0.45	2.9	4.5	1.7	1.0	5.5	5.0			
		Pin				154 T				,		054 T					TEST CURF	RENT	/ VOL1	AGE A	PPLIED	TO P	INS LI	STED	BELOW	/ :		
		Under		5°C		5°C		25°C		°C		25°C		5°C		1	1	1	v	V _{IH}	V	V _{th 1}	v	V	v	V	V _{IHX}	1 !
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	Іон	lin	VIL	V IH	V _R	V th 1	V _{th 0}	V _{out}	V _{cc}	V _{CCH}	* IHX	Gnd
Input Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	14	-	-	-	4	-	-	1,2,3,5,6,7, 8,9,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7,8, 9,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 8,9,10
Breakdown Voltage	BV in "0"	1	5, 5	-	5.5	-	5.5	-	5, 5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 8, 9, 10
	вv _{in''1''}	1	5.5	-	5.5	-	5.5	-	5.5	-	5. 5	-	5.5		Vdc	-	-	1	-	-	-	-	-	-	4	-	_	2,3,5,6,7, 8, 9, 10, 14
Output Output Voltage	V _{out ''0''}	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	1	-	-	4	-	-	2,3,5,6,7, 8,9,10
	v _{out "1"}	11	2. 5	-	2.4	-	2. 5	-	2.5	-	2. 4	-	2.5	-	V dc	-	11	-	-	-	-	-	1	-	4	-	-	2,3,5,6,7, 8, 9, 10
Leakage Current	I _{OLK}	11	-	250	-	250	-	250	-	250	-	250	-	250	μ Adc	-	-	-	-	-	-	-	-	11	4	-	-	1,2,3,5,6,7, 8,9,10,14
Short-Circuit Current	I _{SC}	11	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7, 8,9,10,11, 14
Output Voltage	v _{OL}	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	1	-	-	-	-	4	-	-	2,3,5,6,7, 8,9,10
	v _{он}	11	2. 70	-	3. 10	-	3. 15	-	2.9	-	3.0	-	3.0	-	Vdc	-	11	-	1	-	-	-	-	-	4	-	- ,	2,3,5,6,7, 8,9,10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	17	-	-	-	-	-	18	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7, 8,9,10,14
Power Supply Drain	I _{PDH}	4	-	12	-	12	-	12	-	16	-	16	-	16	mAdc	-	-	-	-	-	-	-	-	1:	4	-	-	10 1,2,3,5,6,7,
	I _{PDL}	4	Ŀ	10	Ľ	10	-	10	Ļ	13		13	-	13	mAdc	-	-	_	_	ļ-	Ŀ			Ļ	"			8,9,10,14
Switching Parameters Turn-On Delay	t _{on}	1,11	-	-	-	12	-	-	-	-	-	12	-	-	ns	Pulse In	Pulse Out	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10
Turn-Off Delay	toff	1, 11	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10
Rise Time	t _r	1, 11	-	-	-	4.5	-	-	-	-	-	4.5	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10
Fall Time	t _f	1, 11	-	-	-	3.0	-	-	-	-	1-	3.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10

^{*} Prime Fan-Out.

TRIPLE 3-INPUT "NAND" GATE

MTTL II MC2100/2000 series

MC2107 · MC2157 MC2007 · MC2057



This device consists of three 3-Input AND gates driving output inverters. These gates can be used to build a pulse shaping network for interfacing with discrete component circuits.

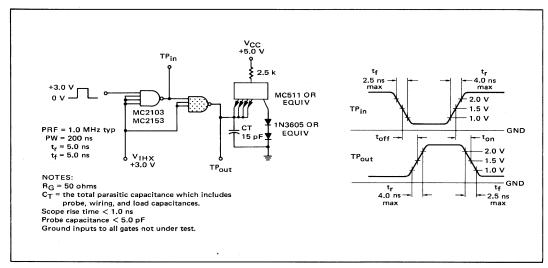


Positive Logic: $5 = \overline{1 \cdot 2 \cdot 3}$ Negative Logic: $5 = \overline{1 + 2 + 3}$

Total Power Dissipation = 66 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SERIES	INPUT LOADING FACTOR	(IF)	OUTPUT DRIVE	=)	(IOL)	TEMPERATURE RANGE
MC2107 MC2157	1	(-2.0 mA)	11 MC2100 series Gates 6 MC2100 series Gates	mA)	(22 mA) (12 mA)	-55°C to +125°C
MC2007 MC2057	1	(-2.5 mA)	9 MC2000 series Gates 5 MC2000 series Gates	mA)	(22.5 mA) (12.5 mA)	0º to +75ºC

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



							TI	ST CO	NDITIO	NS					
				mA							Volts				
	@ Test	I,	DL .	ار	ЭН		VIL	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	V _{cch}	V _{IHX}
Ter	nperature	Pr*	Std	Pr*	Std	lin	, IF	* IH	*R	th 1	*th O	* out	*cc	*ссн	"IHX
	(−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4. 5	2.0	0.9	5.5	5.0	-	-
MC2107*, MC2157	} +25℃	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4. 5	1.7	1.1	5.5	5.0	8.0	3.0
	(+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
MC2007*, MC2057	{ +25℃	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	(+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	_	-

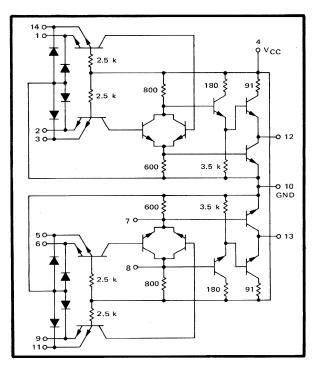
		Pin		C2107	, MC2	157 T	est Li	mits	M	2007	, MC2	057 T	est Li	mits			TEST CURI	RENT	/ VOI 1	ΓAGE A	APPLIED	TO P	INS II	STED	RFIOW	 I ·		
_		Under	-5	55°C	+;	25°C	+1	25°C)°C		25°C		′5°C		<u> </u>	1 .	1 .	· 									4
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	Іон	lin	VIL	V _{IH}	V _R	V _{th 1}	V _{th O}	Vout	V _{cc}	V _{CCH}	V _{IHX}	Gnd†
Input						Г		Γ						Π		Ι	Ι		Γ	T		Γ	T				I	
Forward Current	$^{\mathrm{I}}\mathrm{_{F}}$	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	1 <u>-</u>	-	-	-	2,3		-	-	4	-	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV _{in ''0''}	1	5.5	-	5. 5	-	5.5	-	5.5	-	5. 5	-	5.5	-	Vdc	-	-	1	-	-	-	T -	-	-	4	-	-	10
	BV _{in ''1''}	1	5. 5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10
Output Output Voltage	v _{out ''0''}	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	5	-	-	-	-	-	1	-	-	4	-	-	10
	V _{out ''1''}	5	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	5	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	IOLK	5	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	5	4	-	-	1,2,3,10
Short-Circuit Current	I _{SC}	5	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3, 5,10
Output Voltage	V _{OL}	5	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	5	-	-	-	1	-	-	-	-	4	-	-	10
	V _{OH}	5	2.7	-	3.1	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	5	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	19.5	-	-	-	-	-	20. 25	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,6,10,11
Power Supply Drain	I _{PDH}	4	-	22.5	-	22.5	-	22.5	-	30	-	30	-	'30	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10 ‡
	I _{PDL}	4	-	11.25	-	11.25	-	11.25	-	15	Ξ	15		15	mAdc	-	-	•	-	-	-	-	-	-	4	-	-	1,6,10,11
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	ton	1,5				10			-	-	<u> </u>	10			ns	1	5	-			-	<u> </u>			4	-	2,3	10
Turn-Off Delay	toff	1,5			-	10				-	Ŀ	10	-		ns	1	5	-					-	-	4	-	2,3	10
Rise Time	t _r	1,5	-	-	-	4.0	-	-	-	-	-	4.0			ns	1	5	-	-	-	-	-		-	4		2,3	10
Fall Time	t _f	1,5	-	-	-	2.5	- ₋	-	-	-	-	2.5	-	-	ns	1	5	-	-	-	-	-	-	-	4	-	2,3	10

^{*} Prime Fan-Out † Ground inputs to gates not under test, during ALL tests unless otherwise noted. ‡ The inputs to all gates must be ungrounded.

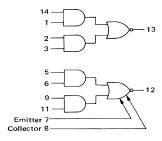
EXPANDABLE DUAL 2-WIDE 2-INPUT "AND-OR-INVERT" GATE

MTTL II MC2100/2000 series

MC2113 · MC2163 MC2013 · MC2063



One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together and driving an output inverter with the ORing nodes made available for expansion. Up to 10 AND gates can be ORed together using the MC2102 or MC2106 expanders series. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



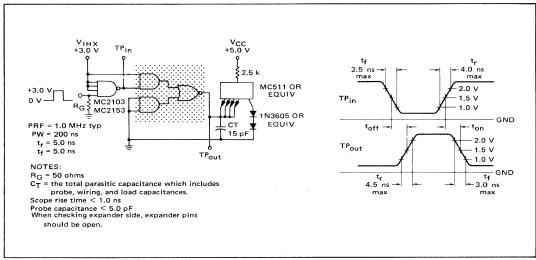
Positive Logic: $13 = \overline{(1 \cdot 14) + (2 \cdot 3)}$ $12 = \overline{(5 \cdot 6) + (9 \cdot 11) + (Expander)}$

Total Power Dissipation = 58 mW typ/pkg Propagation Delay Time = 8.0 ns typ

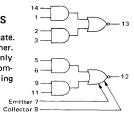
SERIES	INPUT LOADING FACTOR	(IF)	OUTPUT DRIVE	(I _O L)	TEMPERATURE RANGE
MC2113 MC2163	1	(-2.0 mA)	11 MC2100 series Gates 6 MC2100 series Gates	(22 mA) (12 mA)	-55°C to +125°C
MC2013 MC2063	1	(-2.5 mA)	9 MC2000 series Gates 5 MC2000 series Gates	(22.5 mA) (12.5 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



							TI	ST CO	NDITIO	NS					
				mΑ							Volts				
(② Test	ار)L	ار	Н		V _{IL}	v	v	v	V	v	v	V	V
Tem	perature	Pr*	Std	Pr*	Std	l _{in}	* IL	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	V _{CCH}	V _{IHX}
(−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
MC2113*, MC2163	+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1,1	5.5	5.0	8.0	3.0
(+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5. 5	5.0	-	-
	(0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
MC2013*, MC2063	+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

-		Pin				2163				C2013			•		1		TEST CURI	RENT	/ VOL1	AGE A	\PPLIED	TO F	PINS L	ISTED	BELOV	/ /:		1
Characteristic	Symbol	Under Test		55°C May		25°C		25°C Max)°C Max	-	25°C	-	75°C May	Unit	lor	Гон	Iin	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	V _{CCH}	V _{IHX}	Gnd†
		100.	Ivan	Max	74411	ITIOX	/*****	Mux	171111	Midx	74111	Max	1,144111	Max	0	<u> </u>	Un Un	1		<u> </u>			1110	001		ССП	IIIX	- Ond 1
Input Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	14	-	-	-	4	-	-	1,2,3,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-		-	1	-	-	-	4	-	-	2,3,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	ļ -	4	-	-	2,3,10
Breakdown Voltage	BV _{in ''0''}	1	5.5	-	5.5	-	5. 5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	T -	-	4	-	-	2,3,10
	BV in "1"	1	5.5	-	5. 5	-	5.5	-	5. 5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10,14
Output Output Voltage	v _{out ''0''}	13	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	13	-	-	-	-	-	1	-	-	4	-	-	2,3,10
	Vout "1"	13	2.5	-	2.4	+=	2.5	-	2.5		2.4	-	2.5	 -	Vdc	-	13	-	† - -	-	-	†-	1	-	4	-	-	2,3,10
Leakage Current	IOLK	13	-	250	-	250	-	250	-	250	-	250	-	250	μAde	-	-	-	-	-	-	-	<u> </u>	13	4	-	-	1,2,3, 10,14
Short-Circuit Current	I _{SC}	13	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10, 13,14
Output Voltage	V _{OL}	13	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	13	-	-	-	1	-	-	-	† -	4	-	-	2,3,10
	v _{OH}	13	2.7	-	3.1	-	3. 15	-	2.9	-	3.0	-	3.0	-	Vdc	-	13	-	1	-	-	-	-	-	4	-	-	2,3,10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	20	-	-	-	-	-	22	-	-	mAdc	-	-	-	-	-	-	-	-	-	_	4	-	1,2,3, 10,14
Power Supply Drain	I _{PDH}	4	-	18	-	18	-	18	-	24	-	24	-	24	m Adc	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	IPDL	4	-	12	-	12	-	12	-	15	-	15	-	15	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3, 10,14
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	ton	1, 13	-	-	-	11	-	-	-	-	-	11	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Turn-Off Delay	toff	1, 13	-	-	-	11	-	-	-	-	-	11	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Rise Time	t _r	1, 13	-	-	-	4.5	-	-	-	-	-	4.5	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Fall Time	t _f	1, 13	-	-	-	3.0	-	-	-	-	-	3.0	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10

^{*} Prime Fan-Out

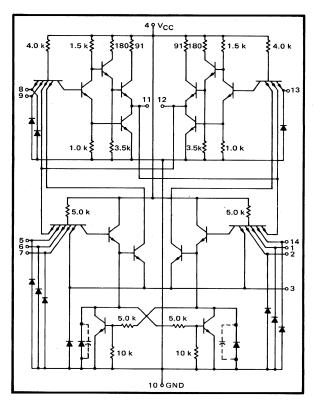
[†] Ground inputs to gates not under test during ALL tests unless otherwise noted.

[‡] The inputs to all gates must be ungrounded.

MTTL II MC2100/2000 series

"AND" J-K FLIP-FLOP

MC2109 · MC2159 MC2009 · MC2059

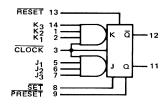


ىن و PRESET

^J1 ⁵ ℃

اء 6 مل اء 7 م The MC2009, MC2059, MC2109, and MC2159 are clocked flip-flops that trigger on the negative edge and perform the JK logic junction. Each flip-flop has an AND input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gates in counters and certain other applications. A direct SET, PRESET, and RESET are also available.

In normal operation, information is changed on the J and K inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory when the clock is in a high state. When the clock returns low, the information is transferred to the bistable section and the Q and $\overline{\mathbf{Q}}$ outputs respond accordingly. The information on the J and K,inputs should not be changed while the clock is high. Each flip-flop can be set or reset directly by the direct $\overline{\mathbf{SET}}$, $\overline{\mathbf{PRESET}}$, or $\overline{\mathbf{RESET}}$ inputs. Since each flip-flop is a charge-storage device, there is a restriction on the clock fall time that must be observed.



EQUIVALENT CIRCUIT	
	○ 13 RESET
	014K3
	1 K ₂ 2 K ₁
	CLOCK

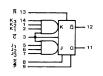
J	κ	a_n	0 _{n+1}
0	0	0	0
0	0	1	1 1
0 0 0	1	0	0
0	1	1	0
1	0	о	1
1	0	1	1
1	1	0	1
1	1	1	0
		-	

Where $J = J_1 \cdot J_2 \cdot J_3$ $K = K_1 \cdot K_2 \cdot K_3$

Total Power Dissipation = 40 mW typ/Pkg Switching Times: ton = 20 ns typ toff = 13 ns typ

SERIES		OADING TOR	(1	F)	OUTPUT DRIVE	(I _{OL})	TEMPERATURE
SETTLES	CLOCK	ALL OTHER	CLOCK	ALL OTHER	OOTTOT BRIVE	('OL'	RANGE
MC2109 MC2159	1.00	0.66	(-2.0 mA)	(-1.33 mA)	11 MC2100 series Gates 6 MC2100 series Gates		-55°C to +125°C
MC2009 MC2059	1.00	0.66	(-2.5 mA)	(-1.66 mA)	9 MC2000 series Gates 5 MC2000 series Gates		0°C to +75°C

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



								TES	T CON	DITIONS				
				m/	\					٧	olts			
	@ Test	ار	DL	Ic	Н	_	21	v	v	v	v	v	Vout	Vcc
Ten	nperature	Pr*	Std	Pr*	Std	lin	2 I _{in}	٧ _{ال}	V _{IH}	V _R	V _{th 0}	V _{th 1}	*out	*cc
	(−55°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2.0	5.5	5.0
MC2109*, MC2159	+25℃	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.2	1.7	5.5	5.0
	(+125°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	0.9	1.4	5.5	5.0
	(0°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.9	5.5	5.0
MC2009*, MC2059	} +25°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0
	(+75°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0

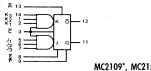
		Pin			<u> </u>	2159 T				C2009,							TEST CU	RRENT	/ VOI	TAGE	APPLI	ED TO PINS	LISTED	BELOW	<i>l</i> :		
Characteristic	Symbol	Under Test		5°C Max		5°C Max		25°C Max		°C Max		5°C Max		75°C Max	Unit	loL	Гон	Iin	2 I _{in}	V _{IL}	V _{IH}	V _R	V _{th 0}	V _{th 1}	V _{out}	V _{cc}	Gnd
Input Forward Current	I _F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	3 -	-1.66	6 mAdo	-	-	-	-	-	-	2,3,5,6, 7,9,13,14	-	-	-	4	1,8,10
		5	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,6, 7,8,9,14	-	-	-		5,10,13
		8	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,13
		9	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,8,14	-	-	-		9,10,13
		13			-		-	 	-	+	-		-	Į Į		-	-	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-	<u> </u>	8,10,13
Leakage Current	I _R	1 5	-	100	-	100	-	100	-	100	-	100	-	100	μAdd	- '	-	-	-	-	-	1 5	-	-		4	2,3,5,6,7,10,11,14 1,2,3,6,7,10,12,14
		8 9 13	-		-		-		-		-		-			-	-	-	-	-	-	9 13	-	-	-		1,2,3,5,6,7,9,10,12,14 1,2,3,5,6,7,8,10,12,14 1,2,3,5,6,7,10,11,14
Inverse Beta Current	IL	1 5	-	100	-	100	-	100	-	100	-	100	-	100	μAdo	-	-	1:	-	8	-	1 5	-	-	-	4	10
		8 9 13	-		-		-		-		-		-			-	-	-	-	1 8	-	8 9 13	-	-	-		
Breakdown Voltage	BV in "0"	1 5	5.5	-	5.5	-	5.5	-	5. 5	-	5.5	-	5.5	<u> </u>	Vdc	-	-	1 5	-	8	-	-	-	-	-	4	10
		8 9 13	l	-				-	$ \downarrow $	-		7		-		-	-	8 9 13	-	V	-	-	-	-	-		
	BV _{in"1"}	1 5 8 9 13	5.5	-	5.5	-	5.5	-	5.5		5. 5		5.5	-	Vdc	- - - -		1 5 8 9 13	-			-		-	-	4	2,3,5,6,7,10,11,14 1,2,3,6,7,10,12,14 1,2,3,5,6,7,9,10,12,14 1,2,3,5,6,7,8,10,12,14 1,2,3,5,6,7,10,11,14

^{*} Prime Fan-Out.

(continued)

ELECTRICAL CHARACTERISTICS (continued) # 13 -

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



						20.0		TES	I CON	IDITIONS		
				m/						٧	olts	
	@ Test	ا	DL .	ار	Н		2 1	.,	,	.,	,	v
Ten	nperature	Pr*	Std	Pr*	Std	lin	2 I _{in}	٧ _{ال}	V _{IH}	V _R	Viho	V _{th 1}
1	_55°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2. 0
159	+25℃	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4. 5	1. 2	1.7
	+125°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0. 45	2.8	4. 5	0.9	1.4
	(0°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4. 5	1.1	1.9
059 -	425°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8

MC2009*, MC20:

+75°C 22.5 12.5 -1.2 -0.6 1.0 2.0 0.45 3.0

Vout

5.5 5.0

5.5 5.0 5.5 5.0 5.5 5.0

5.5 5.0

															. , , , ,	22.0 12.0	2.0	1.0	2.0	0. 10	0.0	4. 3	1.1	1. /	0.0	3.0]
		Pin Under	-5			2159 T !5°C		mits 25°C	M(C2009,		059 T !5°C		imits 75°C			TEST CUI	RRENT	/ VOL	TAGE	APPL	IED TO PINS	LISTED	BELOW	! :		
Characteristic	Symbol	Test				Max									Unit	loL	I _{OH}	l _{in}	2 I _{in}	V _{fL}	V _{iH}	V _R	V _{th O}	V _{th 1}	Vout	V _{cc}	Gnd
Clock Input Forward Current	I _F	3	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	-	1,2,5,6, 7,8,9,13,14	-	-	-	4	3,10
Leakage Current	I_{R}	3	-	150	-	150	-	150	-	150	-	150	-	150	μ A dc	-	-	-	-	-	-	3	-	-	-	4	1,2,5,6,7,10,14
Inverse Beta Current	IL	3	-	200 200	-	200 200	-	200 200	-	200 200	-	200 200	-	200 200	μAdc μAdc	-	-	-	-	13 8	-	3 3	-	-	-	4	10 10
Breakdown Voltage	BV in ''0''	3 3	5. 5 5. 5	-	5.5 5.5	-	5. 5 5. 5	-	5.5 5.5	-	5. 5 5. 5	-	5. 5 5. 5	-	Vdc Vdc	-	-	-	3	13 8	-	-	-	-	-	4 4	10 10
	BV _{in"1"}	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-		3	-	-	-	-	-	-	4	1,2,5,6,7,10,14
Output Output Voltage	v _{out ''0''}	12 11 11	-	0.45	-	0.45	- - -	0.45	-	0.45	- - -	0. 45		0.45	Vdc	12 11 11	- - -	-	-	-	-	-	-	13 9 8	-	4	3,8,10 3,10,13 3,10,13
	v _{out} ''1''	12 11 11	2.5	-	2.4	-	2.7	-	2.5		2. 4	-	2.5	-	Vdc	- - -	12 11 11	-	-		-		13 9 8	-	-	4	8,10 10,13 10,13
Leakage Current	I _{OLK}	12 11	-	225 225	-	225 225	-	225 225	1 1	225 225	-	225 225	-	225 225	μAdc μAdc	-	-	-	-	-	-	-	-	-	12 11	4	1,2,3,5,6,7,8,9,10,13,14 1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	I _{SC}	12 11	-	-	-30 -30	-70 -70	-	-	1 1	1 1	-30 -30	-70 -70	-	-	mAdc mAdc	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,12,13,14 1,2,3,5,6,7,8,9,10,11,13,14
Output Voltage	V _{OL}	12 11 11	-	0. 40 . ↓	-	0.40	-	0. 45		0.40		0.40	-	0.45	Vdc	12 11 11	-	-	-	-	13 9 8		-	-	-	4	3,8,10 3,10,13 3,10,13
	v _{ОН}	12 11 11	2.80	-	3. 20	-	3.35	-	3.00		3. 10	-	3. 15	-	Vdc	- - -	12 11 11	-	-	13 9 8	-	-	-	-	-	4	8,10 10,13 10,13
Power Requirements (Total Device) Power Supply Drain	I _{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	mAdc	-	-	-	_	-	-	-	-	-	_	4	3,10,13
	I_{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	mAde	-	-	-	-	-	-	-	-	-	-	4	3,8,10

^{*} Prime Fan-Out.

MC2109, MC2159/MC2009, MC2059 (continued)

OPERATING CHARACTERISTICS

Clock fall time ≤ 100 ns.

Triggers on clock pulse widths \geq 15 ns.

Provides direct SET, PRESET, and RESET inputs. The application of a "0" state to 8 or 9, sets Q high; "0" state to 13, resets Q low. The clock must be in the low state when these functions are performed.

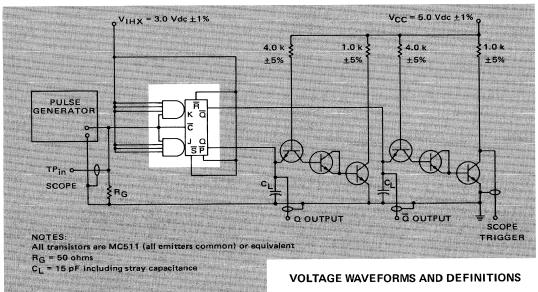
Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1"

state to "0" state information change on the J and K terminals. The flip-flop will require typically 6.0 ns to recognize a "0" state to "1" state change.

Negative edge triggering — When the clock goes from the high state to the low state, the information in the temporary storage section is transferred and the Ω and $\overline{\Omega}$ outputs will respond accordingly. While the clock is in a low state, the J and K terminals are inhibited.

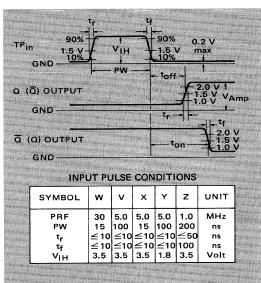
Unused J and K inputs should be tied to the clock or to 2.0 to 5.0 Vdc. $\overline{\text{PRESET}}$ and $\overline{\text{SET}}$ are tied to $\overline{\Omega}$; $\overline{\text{RESET}}$ is tied to Ω .

FIGURE 1 - SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	toff	Visite Visites		20	ns
Delay Time On	ton	V	***************************************	25	ns
Rise Time	tr	V	A Property	6.0	ns
Fall Time	the tr	V		4.0	ns
Amplitude	VAmp	v	3.2	Sec. 1	Volt
(Devîce	WORST-C must toggle			oulse)	T.
TEST	SYMBO	L LIMI	TS (INP CONDI	
Toggle Frequenc	y frog	30 MH	zmax	**** V	r.
Pulse Width	PW	15 ns n	nin	×	Section 1
Input High Volta	ge VIH	1.8 V r	nin,	Y	
Fall Time	te	100 ns	max	administracy	30



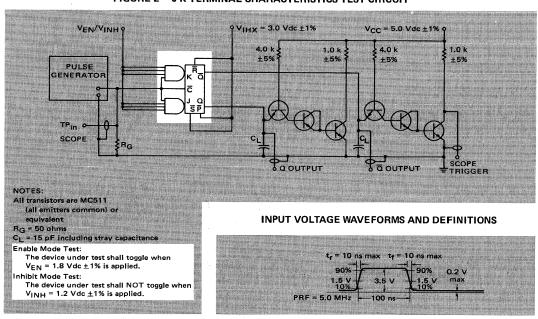
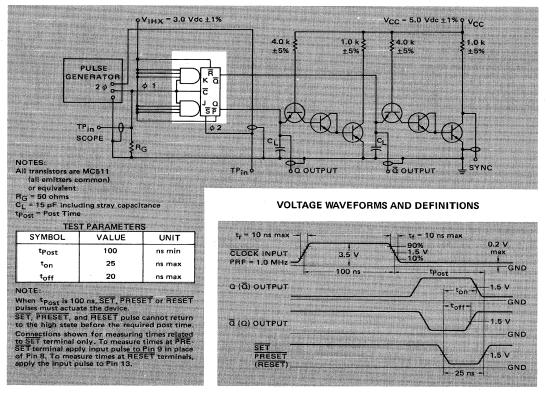


FIGURE 2 - J-K TERMINAL CHARACTERISTICS TEST CIRCUIT

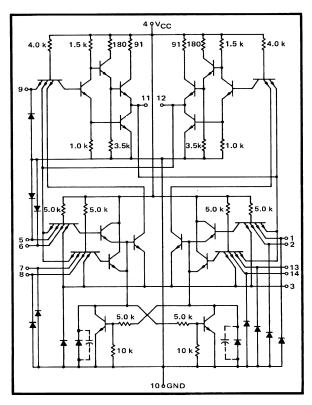
FIGURE 3 - SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT



MTTL II MC2100/2000 series

"OR" J-K FLIP-FLOP

MC2110 · MC2160 MC2010 · MC2060

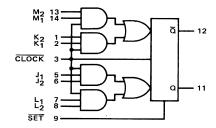


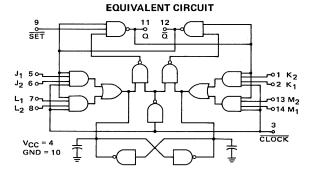
The MC2110, MC2160, MC2010, and MC2060 are clocked flip-flops that trigger on the negative edge and are internally wired to perform the J-K logic function. Each flip-flop has a positive logic AND-OR input gating configuration that consists of two clocked J inputs ANDed together, two clocked K inputs ANDed together, two clocked L inputs ANDed together, and two clocked M inputs ANDed together. The J and the L inputs are ORed together and the K and the M inputs are ORed together. A direct SET is also available.

In normal operation, information is changed on the clocked inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory through the AND-OR input gating when the clock is in the high state. When the clock returns low the information in the temporary memory is transferred to the bistable section and the Q and the Q outputs respond accordingly. The information on the clocked inputs should not be changed while the clock is high.

Each flip-flop can be set directly by applying a low state to the direct SET input. Since each flip-flop is a charge storage device there is a restriction on the clock fall time that must be observed.

The AND-OR input configuration of each flip-flop makes it very useful for shift right/shift left registers and for up/down counters.





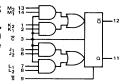
J	L	К	М	Q _n	Q _{n+1}	
0	0 X	×	×	0	0	X = Don't Care Where $J = J_1 \cdot$
× × ×	1 X X X	X X 0 1 X	X 0 X 1	0 1 1 1	1 1 0 0	$ \begin{array}{c} L = L_1 \bullet \\ K = K_1 \bullet \\ M = M_1 \bullet \end{array} $

Total Power Dissipation = 50 mW typ/Pkg Switching Times: ton = 20 ns typ toff = 13 ns typ

SERIES		OADING TOR	(1	F)	OUTPUT DRIVE	(I _{OL})	TEMPERATURE
SERIES	CLOCK	ALL OTHER	CLOCK	ALL OTHER	001101311102	(IOL)	RANGE
MC2110 MC2160	2.00	0.66	(-4.0 mA)	(-1.33 mA)	11 MC2100 series Gates 6 MC2100 series Gates		-55°C to +125°C
MC2010 MC2060	2.00	0.66	(-5.0 mA)	(-1.66 mA)	9 MC2000 series Gates 5 MC2000 series Gates		

ELECTRICAL CHARACTERISTICS Ma 12=

Test procedures are shown for only one J, $\frac{\kappa_1^2}{c}$ one K, and the \overline{SET} input. The remaining $\frac{\kappa_2^2}{c}$ 3 J, K, L, M inputs are tested in the same manner.



ā-12
α 11

(@ Test	ī
Ten	nperature	Pr*
1	_55°C	22.0
MC2110*, MC2160	+25℃	22.0
	(+125°C	22.0
	(0°C	22.5
MC2010*, MC2060	₹ +25°C	22. 5

								TEST	COND	ITION:	S				
					mA							Volts			
. '	@ Test	١ _c)L	ار	Н										
en	nperature	Pr*	Std	Pr*	Std	l _{in}	2 I _{in}	4 I _{in}	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th O}	Vout	٧ _{cc}
1	_55°C	22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
) (+25°C	22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
	+125°C	22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
	(0°C	22.5	12.5	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
)	+25℃	22.5	12.5	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0
	(+75°C	22.5	12.5	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4. 5	1.7	1.1	5.5	5.0
														-	

MC20	10*,	MC2060

		- n		400111		1/0 7				400070	1100	0/0 T			773 C	22.0 122.0	-1.2 -0.0	12.0		1.0	0. 10	0.0	4. 5	1	1.1	0.0	0.0	-
	1	Pin				160 Te				AC2010					1		TEST CUR	RENT	/ VOL	TAGE	APPL	IED T	O PINS LIST	TED BEL	LOW:			
Characteristic	Symbol	Under Test		5°C Max		5°C Max		25°C		°C May		25°C Max		75°C Max	Unit	lou	loh	l:	2 1.	4 I _{in}	٧,,	VIH	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	Gnd
	1	1631	Min	MIGX	Will	IVIdX	MIII	Max	Min	MdX	Will	Max	ING	Max	Unin		-OH	'in	- 'in	in	1 "IL	·IH	· R	1111	- 1110	· out	. CC	Ona
Input Forward Current	I _F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	- ,	-	-	-	2,3,5,6,7, 8,13,14	-	-	-	4	1,9,10
		5	-		-		-		-		-		-			-	-	-	-	-	-	-	1,2,3,6,7, 8,13,14	-	-	-		5,10,11
		9	_	+	-	+	-	•	-	•	-	1	-	+		-	_	-	-	_	-	-	1,2,5,6,7, 8,13,14	-	-	-	1	3,9,10,11
Leakage Current	I _R	1 5 9	=	100	-	100	-	100	- -	100	-	100	-	100	μAdc ↓	- -	-		- -	-	-	-	1 5 9	-	-	-	4 ↓	2,3,5,6,7,8,10,11,13,14 1,2,3,6,7,8,9,10,12,13,14 1,2,3,5,6,7,8,10,12,13,14
Inverse Beta Current	IL	1 5 9	=	100	:	100	- -	100	-	100	-	100	-	100	μAde	-	-	-	-	-	-	-	1 5 9	-	-	-	4	9,10 10,11 10,11
Breakdown Voltage	BV _{in "0"}	1 5 9	5.5	-	5.5	-	5.5	-	5.5	-	5. 5	-	5. 5	:	Vdc	-	-	1 5 9	-	=	-	-	-	-	-	-	4	9,10 10,11 10,11
	BV _{in} "1"	1 5 9	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5. 5	<u>:</u>	Vdc	= -	-	1 5 9	-	=	-	-	-	-	=	-	4	2,3,5,6,7,8,10,11,13,14 1,2,3,6,7,8,9,10,12,13,14 1,2,3,5,6,7,8,10,12,13,14
Clock Input Forward Current	I _F	3	-	-4.0	-	-4.0	-	-4.0	-	-5.0	-	-5.0	-	-5.0	mAdc	-	-	-	-	-	-	-	1,2,5,6,7, 8,13,14	-	-	-	4	3,10
Leakage Current	I _R	3	-	300	-	300	-	300	-	300	-	300	-	300	μAdc	-	-	•	-	-	-	-	3	-	-	-	4	1,2,5,6,7,8,10,13,14
Inverse Beta Current	IL	3 3	-	400 400	-	400 400	-	400 400		400 400	-	400 400	-	400 400	μAdc μAdc	-	-		11	-	-		3 3	-	-	-	4 4	9,10 10,11
	вv _{in ''0''}	3 3	5.5 5.5	-	5. 5 5. 5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	Vdc Vdc	-	-	-	-	3	-	-	-	-	-	-	4	10, 11 10, 12
	BV _{in"1"}	3	5.5	-	5.5	<u> </u>	5. 5	-	5.5	-	5. 5	-	5. 5		Vdc	-	-	-	3		-		-	-	-	-	4	1,2,5,6,7,8,10,13,14
Output (For Set Only) Output Voltage	v _{out "0"}	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11①	-	-	-	-	-	-	-	9	-	-	4	3, 10
	V _{out "1"}	11	2,5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	11	-	-	-	-	_	-	-	9	-	4	3,10
Leakage Current	IOLK	12 11	-	650 650	-	650 650	-	650 650	- -	650 650	-	650 650	-	650 650	μAdc μAdc	-	-	-		-	-	1.1	12 11	-	-	-	4	1,2,3,5,6,7,8,10,11,13,14 1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	I _{SC}	12 11	-	<u> </u>	-30 -30	-70 -70	-	-	-	-	-30 -30	-70 -70	-	-	mAdc mAdc	-	-	-	-	-	-	1 1	-	-		-	4	1,2,3,5,6,7,8,10,11,12,13,14 1,2,3,5,6,7,8,9,10,11,13,14
Output Voltage	v _{он}	12 11	2.80 2.80		3.20 3.20	-	3.35 3.35	-	3.00 3.00	-	3.10 3.10	-	3. 15 3. 15	-	Vdc Vdc	-	12 11	-	-	-	-	-	-	-	-	-	4	3,10,11 3,10,12
	V _{OL}	12 11	-	0. 40 0. 40	-	0.40 0.40	-	0.45 0.45	-	0.40 0.40	-	0.40 0.40	-	0.45 0.45	Vdc Vdc	12① 11①	-	-	:	:	-	9	-	-	-	-	4	3,10 3,10
Breakdown Voltage	Io	12 11	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	mAde mAde	- '	-	-	:	-	-	-	-		-	12 11	4	1,2,3,5,6,7,8,10,11,13,14 1,2,3,5,6,7,8,9,10,13,14
Power Requirements (Total Device)	١.	١.	_	15		15	_	15		10				,,														
Power Supply Drain	I _{PD}	4	_	15	-	15	-	15 15	-	18 18	-	18 18	-	18 18	Vdc Vdc	-	-	-	-	-		-	-	-	-	-	4	3,10,12 3,10,11

MC2110, MC2160/MC2010, MC2060 (continued)

OPERATING CHARACTERISTICS

Clock fall time ≤ 100 ns.

Triggers on clock pulse widths ≥ 15 ns.

The application of a "0" state to the $\overline{\text{SET}}$ will cause Q to go to the "1" state. The clock must be in the low state when this function is performed.

Data at the clocked inputs must be present before the clock goes to a high state. If the information on the clocked inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1" state to "0" state change. The flip-flop will also require typically 6.0 ns to recognize a "0" state to "1" state change.

Negative edge triggering — When the clock goes from the high state, the information in the temporary storage section is transferred; and the Ω and $\overline{\Omega}$ outputs will change accordingly. While the clock is in a low state, the J, K, L, and M terminals are inhibited.

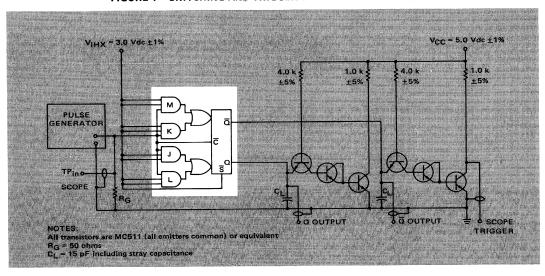
Unused Inputs:

Single unused J, K, L, and M inputs should be tied to the used input, to the clock input, or to 2.0 to 5.0 Vdc.

If both J, K, L, or M inputs are unused, they MUST be tied to ground.

Unused \overline{SET} is tied to \overline{Q} .

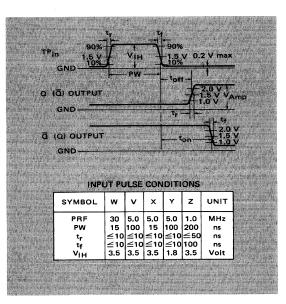
FIGURE 1 - SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	toff.	V		20	ns
Delay Time On	ton	v		25	ns .
Rise Time	9	\ v		6.0	198
Fall Time	4	V		4.0	i ms
Amplitude	VAmp	V	3.2		Volt
(Device	WORST-C must toggle			outse)	
TEST	SYMBO	L LIMI	TS ,	INP CONDI	
Toggle Frequenc	Y ^f Tog PW	30 MH 15 ns n	200	Y	•
Input High Volt Fall Time	age VIII	1.8 V r			

VOLTAGE WAVEFORMS AND DEFINITIONS



MC2110, MC2160/MC2010, MC2060 (continued)

FIGURE 2 – J-K-L-M TERMINAL CHARACTERISTICS TEST CIRCUIT

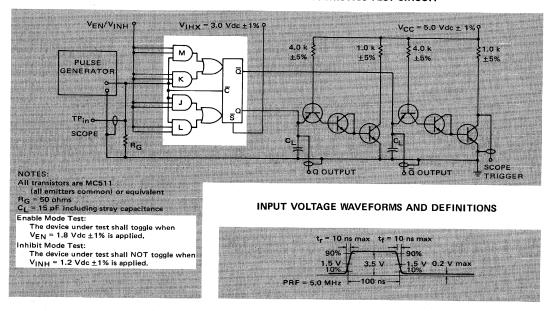
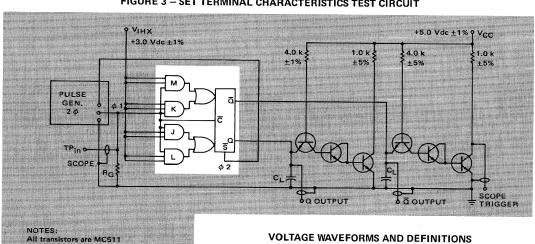


FIGURE 3 – SET TERMINAL CHARACTERISTICS TEST CIRCUIT



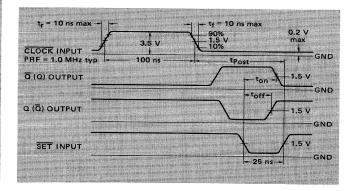
All transistors are MC511 (all emitters common) or equivalent R_G = 50 ohms
C_L = 15 pF including stray capacitance capacitance tpost = Post Time

TEST PARAMETERS

SYMBOL	VALUE	UNIT
^t Post	100	ns min
^t on	25	ns max
t _{off}	20	ns max

NOTE:

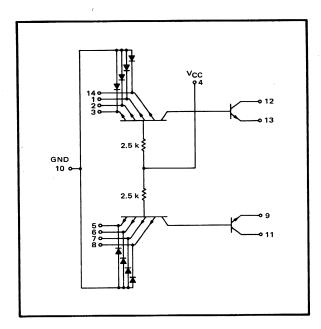
When tpost is 100 ns, SET pulse must actuate the device. SET pulse cannot return to the high state before the required post time.



DUAL 4-INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL II MC2100/2000 series

MC2106 · MC2156 MC2006 · MC2056



This device consists of two independent 4-input AND gates. The outputs of each gate are made available as ORing nodes. Using the MC2102 series and the MC2106 series with any one of the basic expandable gates, up to 10 AND gates can be ORed together.



Total Power Dissipation = 14 mW typ/Pkg.

Propagation Delay Times:

 Δt_{pd} = +1.0 ns typ When added to the expandable AND-OR-INVERT gates.

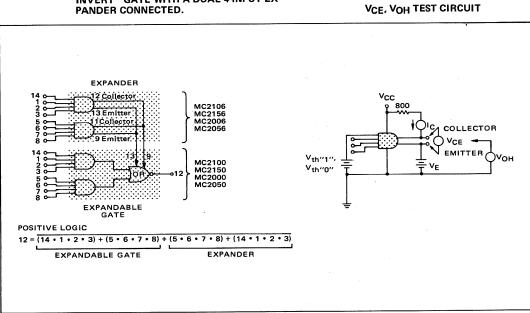
Δt_{pd}/pF = +0.7 ns/pF typ
Caused by additional capacitance at expansion points.

SERIES	INPUT LOADING FACTOR	(IF)	TEMPERATURE RANGE
MC2106 MC2156	1	–2.0 mA	-55°C to +125°C
MC2006 MC2056	1	-2.5 mA	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 2-WIDE 4-INPUT, "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EX-

PANDER CONNECTED.



Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



-						TEST	CON	DITION	VS.				
@ Test	n	ıΑ		-				Volt	rs				
mperature	lc	lin	V _R	VEI	V _{E2}	V _{E3}	V _{th 1}	V _{th O}	V _{out}	V _{CR}	V _{CRH}	V _{cc}	V _{CCH}
(−55°C	6.0	1.0	4.5	1.00	0.90	0.8	2.0	0.9	5.5	*	-	5.0	-
₹ +25°C	6.0	1.0	4.5	0.85	0.75	0.8	1.7	1, 1	5.5	*	**	5.0	8.0
+125°C	6.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-
(0°C	6.0	1.0	4.5	0.90	0.80	0.8	1.9	1.0	5.5	*	-	5.0	-
{ +25℃	6.0	1.0	4.5	0.85	0. 75	0.8	1.8	1.1	5.5	*	**	5.0	7.0
(+75°C	6.0	1.0	4.5	0.75	0.65	0.8	1.7	1.0	5.5	* -	-	5.0	-
	+25°C +125°C 0°C +25°C	nperature I _C -55°C 6.0 +25°C 6.0 +125°C 6.0 +25°C 6.0		nperature I _C I _{in} V _R (-55°C 6.0 1.0 4.5 +25°C 6.0 1.0 4.5 +125°C 6.0 1.0 4.5 +25°C 6.0 1.0 4.5 +25°C 6.0 1.0 4.5	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

									,						750					0.00	Ι	1	1 0	0.0	1	1	J. U	-	
		Pin.			MC2	156 Te	st Lin	nits	MC	2006,	MC2	056 T	est Li	mits			Т	ECT CI	IDDEN	T / VC	NTAC	E ADD	HIED 1	ro DIN	C LICT	TD DEL	014		1
		Under	-5	5°C	+2	25°C	+1	25°C	. 0)°C	+2	25°C	+7	′5°C		w 7	1	E31 ((JKKEN	I / VC	LIAG	E APP	LIED	U PIN	2 1121	ED BEL	UW:]
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	l _c	l _{in}	V _R	V _{E1}	V _{E2}	V _{E3}	V.,,	V _{th O}	Vout	V _{CR}	VCRH	Vcc	V _{CCH}	Gnd [†]
Input											Ī						T				1	1			-	CKII		CCIT	
Forward Current	$I_{ m F}$	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-		2,3,14	-	-	-	-	-	-	- :	-	4	-	1,10
Leakage Current	I _R	1	1	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1		-		-	٠-		-	-	4	-	2,3,10,14
Inverse Beta Current	I _L	1	1	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	13	-	-	-	-	-	12	-	4	-	10 .
Breakdown Voltage	BV in ''0''	1	5.5	-	5. 5		5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	13	-	-	-	-	-	12	-	4	-	10
	вv _{in''1''}	1	5.5	-	5.5	-	5.5	· -	5.5	-	5.5	-	5.5	-	Vdc	-	1		-	-	-	-	-	-	-	-	4	-	2,3,10,14
Output																							_	_					
Output Voltage	· v	12	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	Vdc	-	-	-	-	13	-	-	1	_	12	_	4	l _	10
	v _{CE} ①	12	-	0.65	-	0. 65	-	0.65	-	0. 65	-	0. 65	-	0.65	Vdc	12	-	-	13	-	-	1	-	-	-	-	4	-	10
Leakage Current	I _{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	13	-	-	12	-	-	4	-	1,2,3,10,14
Power Requirements																					_								
(Total Device)	•		.																									1	
Maximum Power Supply Current	I _{max} ②	4	-	-	-	7.0	-	-	7-		-	7.5	-	-	m Adc	-	-	-	-,	-	9,13	-	-	-	-	11, 12	-	4	1,2,3,10,1
Power Supply Drain	I _{PDH}	4	-	3.0	-	3.0	-	3.0	-	3.6	-	3.6	-	3.6	mAdc	-	-	-	-	-	9,13	-	-	-	-	-	4	-	10‡
	I _{PDL}	4	-	4. 25	_	4. 25	-	4. 25	-	5. 25	-	5. 25	-	5. 25	m Adc	-		-	-	-	-	-7.		·		-	4	-	1,2,3,10,14

^{*} Indicated pins tied to $V_{\mbox{\footnotesize{CC}}}$ thru $\,$ 800 ohms $\,$ $_{\mbox{\footnotesize{\pm}}}$ 1.0% resistor.

^{**} Indicated pins tied to V_{CCH} thru 800 ohms \pm 1.0% resistor.

[†] Ground inputs to gate not under test during ALL tests, unless otherwise noted.

[†] The inputs of both gates must be ungrounded.

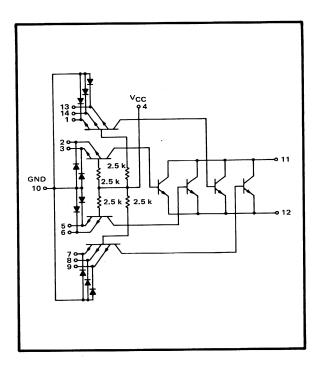
① VCE is referenced to the emitter voltage (Pin 13). The other gate is referenced to (Pin 9).

² Pin 9 ties to Pin 13. Pin 12 ties to Pin 11.

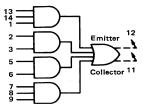
4-WIDE 3-2-2-3 INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL II MC2100/2000 series

MC2102 · MC2152 MC2002 · MC2052



This device consists of two 2-input and two 3-input AND gates ORed together with the common ORing nodes made available as the output. The basic expandable gate can be expanded up to 10 AND gates by using the MC2102 series or the MC2106 series expander package.



Total Power Dissipation = 28 mW typ/Pkg. Propagation Delay Times: Δt_{pd} = +2.0 ns typ When added to the expandable AND-OR-INVERT gates. $\Delta t_{pd}/pF = +0.7 \text{ ns/pF typ}$ Caused by additional capacitance

INPUT LOADING FACTOR TEMPERATURE RANGE SERIES (IF) MC2102 MC2152 -55°C to +125°C -2,0 mA MC2002 MC2052

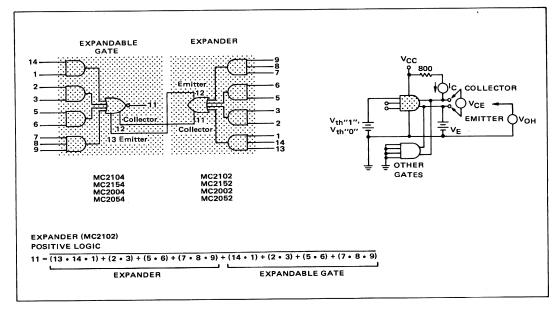
at expansion points.

-2.5 mA Full output loading factor of the expandable gate is maintained.

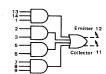
0°C to +75°C

APPLICATION: EXPANDABLE 4-WIDE "AND-OR-INVERT" GATE WITH A 4-WIDE 3-2-2-3 INPUT EX-PANDER CONNECTED.

VCE, VOH TEST CIRCUIT



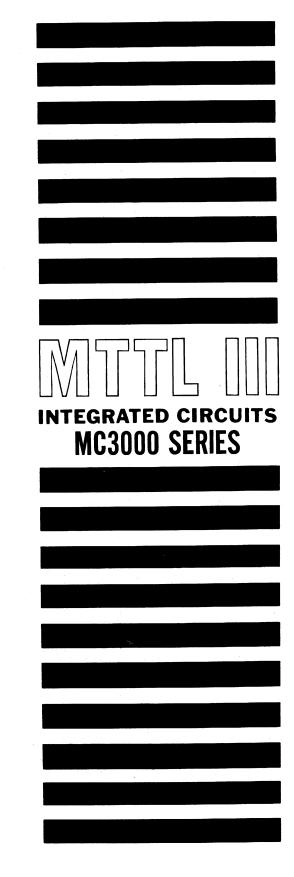
Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



		L				. 1	EST C	ONDIT	IONS					
	@ Test	m	Α						Volts					
Te	mperature	lc	l _{in}	V _R	V _{E1}	V _{E2}	V _{E3}	V _{th 1}	V _{th 0}	Vout	$V_{\rm CR}$	V _{CRH}	V _{cc}	V _{CCH}
	(−55°C	6.0	1.0	4. 5	1.00	0. 90	0.8	2.0	0.9	5. 5	*	-	5.0	-
MC2102 , MC2152	} +25℃	6.0	1.0	4.5	0.85	0. 75	0.8	1.7	1.1	5.5	*	**	5.0	8.0
	(+125℃	6.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-
	(0°C	6.0	1.0	4.5	0.90	0.80	0.8	1.9	1.0	5.5	*	-	5.0	-
MC2002 [°] , MC2052	{ +25℃	6.0	1.0	4.5	0.85	0.75	0.8	1.8	1.1	5.5	*	**	5.0	7.0
	\ +75℃	6.0	1.0	4.5	0.75	0.65	0.8	1.7	1.0	5.5	*	-	5.0	-

														, (+75℃	6.0	1.0	4.5	0.75	0.65	0.8	1.7	1.0	5.5	*	-	5.0	-	
		Pin				2152 T						052 T	est Li	mits				EST CURR	FNT /	VOLT	AGF A	PPI IFI	D TO	PINS I	ISTED	REIOW	۱ <u>. </u>		
Chaman to	١	Under		55°C		25°C		25°C)°C	+	25°C	+7	′5°C		L.								,					
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	l lc	lin	V _R	VEI	V _{E2}	V _{E3}	V _{th 1}	V _{th 0}	Vout	VCR	VCRH	Vcc	V _{CCH}	Gnd
Input Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	m Adc	-	-	2,3,5,6,7, 8,9,13,14		-	-	-	-	-	-	-	4	-	1,10
Leakage Current	IR	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8, 9,10,13,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	12	-		-	-	-	11	-	4	-	2,3,5,6,7,8,9,10
Breakdown Voltage	BV in "0"	1	5.5	-	5.5	-	5.5	-	5. 5	1	5.5	-	5.5	-	Vdc	-	1	-	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10
	вv _{in''1''}	1	5.5	_	5.5		5.5	-	5.5	_	5.5	-	5.5	-	Vdc	_	1	-	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8,9, 10,13,14
Output Voltage	v _{OH} v _{CE} ①	11 11	4.8	- 0. 65	4.8	- 0.65	4.8	- 0. 65	4.8	0.65	4.8	- 0. 65	4.8	-	Vdc	-	-	-	-	12	-	-	1	-	11	-	4	-	2,3,5,6,7,8,9,10
	CE		<u> </u>			0.00		0.03		0.03		0.65		0.65	Vdc	11		-	12	<u> </u>	-	1	-		-	-	4	-	2,3,5,6,7,8,9,10
Leakage Current	IOLK	11	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	·-	12	-	-	11	-	-	4	-	1,2,3,5,6,7,8, 9,10,13,14
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-		14	-	-	-	-	-	15	-	-	mAdc	-		-	-	-	12	-	-	-	-	11	-	4	1,2,3,5,6,7,8, 9,10,13,14
Power Supply Drain	I _{PDH}	4	-	6. 0 8. 5	-	6.0	-	6.0	-	7. 2	-	7. 2	-	7.2	mAde	-	-	-	-	-	12	-	-	-	-	-	4	-	10
	PDL	*	_	8.5	-	8.5	-	8.5	-	10.5	_	10.5	-	10. 5	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8, 9,10,13,14

^{*} Indicated pins tied to V_{CC} thru 800 ohms $\pm 1.0\%$ resistor. ** Indicated pins tied to V_{CCH} thru 800 ohms $\pm 1.0\%$ resistor. ① V_{CE} is referenced to the emitter Voltage (Pin 12).



INTEGRATED CIRCUITS

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NUMERICAL INDEX (Functions and Characteristics)

 $V_{CC} = 5.0 \text{ V}, T_A = 25^{\circ}\text{C}$

Function	Type	Output Loading Factor Each Output	Propagation Delay ^t pd ns typ	Power Dissipation mW typ/pkg	Page No.
Quad 2-Input NAND Gate	MC3000	10	6.0	88	4-112
Quad 2-Input AND Gate	MC3001	10	9.0	112	4-110
Quad 2-Input NOR Gate	MC3002	10	6.0	122	4-114
Quad 2-Input OR Gate	MC3003	10	9.0	150	4-116
Triple 3-Input NAND Gate	MC3005	10	6.0	66	4-108
Dual 4-Input NAND Gate	MC3010	10	6.0	44	4-104
Single 8-Input NAND Gate	MC3015	10	8.0	22	4-102
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC3020	10	6.0	62.5	4-106
Dual 4-Input NAND Power Gate	MC3025	20	6.0	70	4-120
Dual 4-Input AND Power Gate	MC3026	20	9.0	90	4–118
Dual 3-Input 3-Output AND Series Terminated Line Driver	MC3028	*	9.0	56	4-124
Dual 3-Input 3-Output NAND Series Terminated Line Driver	MC3029	•	6.0	44	4-126
Dual 4-Input Expander for AND-OR-INVERT Gates	MC3030	**	***	15	4-122
AND J-K Flip-Flops	MC3050	10	f = 40 MHz	80	4–128
AND Input JJ-KK Flip-Flop	MC3052	10	f = 40 MHz	75	4-133
Dual Type Ď Flip-Flop	MC3060	10	f = 30 MHz	120	4-138
Dual J-K Flip-Flop	MC3061	10	f = 50 MHz	100	4-141
Dual J-K Flip-Flop	MC3062	10	f = 50 MHz	100	4-145

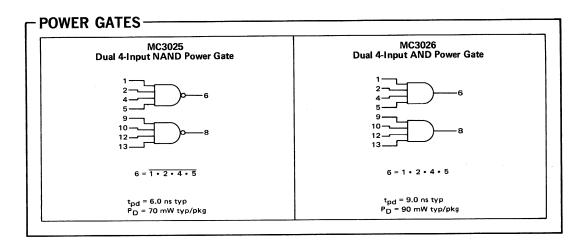
^{*}Direct Output = 10 minus the number of resistor-terminated outputs being used.

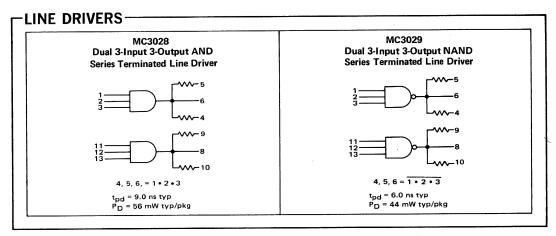
^{**}Full output loading factor of the expandable gate is maintained.

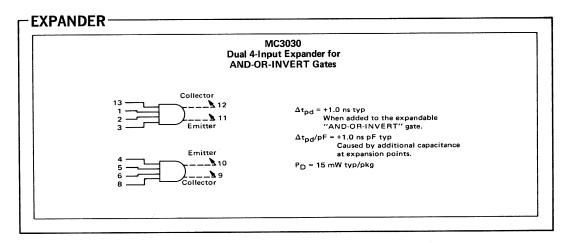
^{***} Δt_{pd} = +1.0 ns typ when added to the expandable AND-OR-INVERT Gate.

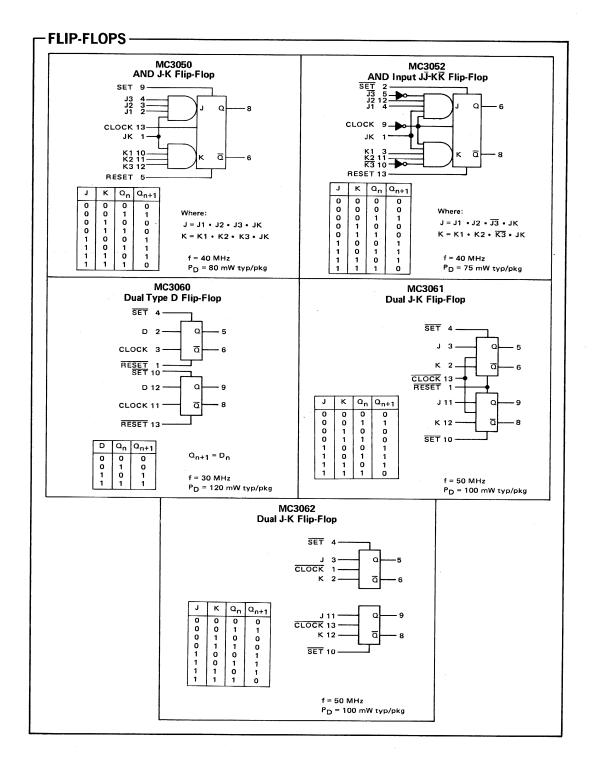
 $[\]Delta t_{pd}/pF$ = +1.0 ns pF typ caused by additional capacitance at expansion points.

-GATES MC3000 MC3001 MC3002 Quad 2-Input NAND Gate **Quad 2-Input AND Gate Quad 2-Input NOR Gate** 10 10 12 12. 13 13. 3=1.2 3 = 1 • 2 $3 = \overline{1 + 2}$ t_{pd} = 6.0 ns typ P_D = 88 mW typ/pkg t_{pd} = 9.0 ns typ P_D = 112 mW typ/pkg t_{pd} = 6.0 ns typ P_D = 122 mW typ/pkg MC3003 MC3005 MC3010 **Quad 2-Input OR Gate Triple 3-Input NAND Gate Dual 4-Input NAND Gate** 10 12 13 3 = 1 + 212 = 1 • 2 • 13 6 = 1 • 2 • 4 • 5 t_{pd} = 9.0 ns typ P_D = 150 mW typ/pkg t_{pd} = 6.0 ns typ P_D = 44 mW typ/pkg $t_{pd} = 6.0 \text{ ns typ}$ $P_D = 66 \text{ mW typ/pkg}$ MC3015 MC3020 Single 8-Input NAND Gate Expandable Dual 2-Wide 2-Input **AND-OR-INVERT Gate** 10 Emitter 11 Collector 12 8 = 1 • 2 • 3 • 4 • 10 • 11 • 12 • 13 $8 = (9 \cdot 10) + (13 \cdot 1) + (Expanders)$ t_{pd} = 8.0 ns typ P_D = 22 mW typ/pkg $t_{pd} = 6.0 \text{ ns typ}$ $P_D = 62.5 \text{ mW typ/pkg}$











GENERAL INFORMATION SECTION

INTRODUCTION

MTTL III integrated circuits are designed with speed approaching the limit for saturated logic and for good load driving capability. This line includes all the characteristics that have made transistor-transistor logic so popular. The major advantage of MTTL III over other TTL lines is the square transfer characteristic (Figure 1) that exists only for the MTTL III family. Because of this "ideal" transfer characteristic, the MTTL III family is the only TTL line that is truly compatible with MDTL. Another advantage of this family over competitive TTL lines is that it is designed to minimize problems associated with ringing.

The circuits in the MTTL III family are distinguished by a multiple-emitter input transistor, a darlington active "pull-up" in the upper output network, and an active bypass network in the base of the output pull-down transistor as shown in Figure 2.

The multiple-emitter input configuration offers the maximum logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The

Darlington output configuration provides very low output impedances in each of the two output states. These low impedances result in excellent ac noise immunity and allows high-speed operation while driving large capacitive loads.

The active bypass shown in the dotted area of Figure 2 holds the phase inverter transistor "off" until gate threshold is reached. This circuit operation provides the squared transfer characteristic shown in Figure 1.

In addition to improving the transfer characteristic, the bypass network offers a number of advantages compared to a simple resistor that can be traced to a much smaller impedance variation with temperature.

- Lower bypass impedance for the reverse current of the output transistor at elevated temperatures, provides faster turn-off.
- A lower current spike during the turn-off transient causes a lower ac power factor resulting in a lower total power consumption. This advantage is even more pronounced at higher temperatures.
- 3. Faster turn-on at low temperature.

FIGURE 1 — COMPARISON OF CONVENTIONAL TRANSISTOR-TRANSISTOR LOGIC AND MTTL III

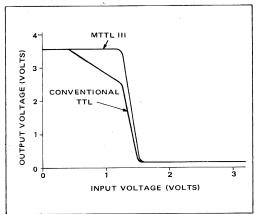
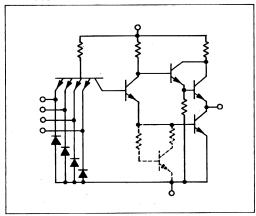


FIGURE 2 - TYPICAL MTTL III CIRCUIT





GENERAL INFORMATION SECTION

TYPICAL CHARACTERISTICS

Typical operating characteristics of the MTTL III family include: (Unless otherwise indicated, the parameters are defined for VCC = +5.0 volts and T_A = +25°C.)

Supply Voltage Operating Range = 4.5 to 5.5 volts

Operating Temperature Range: MC3000 Series

0 to +75°C

Output Drive Capability Gates (Output Loading Factor):

MC3000 Series = 10 Gates.

Capacitance = 600 pF

Output Impedance

High State = 10 ohms nominal (unsaturated)

Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits

+5.5 volts maximum

-1.5 volts minimum (1)

Switching Threshold = 1.5 volts nominal

Input Impedance

High State = 400 k ohms nominal

Low State = 2.4 k ohms nominal

Worst-Case do Noise Margin

High State = 0.700 volt minimum Low State = 0.700 volt minimum

Power Dissipation

22 mW per gate typical

50-80 mW per flip-flop typical

Average Propagation Delay = 6.0 ns per gate typical

13 ns per flip-flop typical

Rise Time = 1.0 ns typical

Fall Time = 1.3 ns typical

Flip-Flop Clock Frequency (MC3061) = 50 MHz maximum.

- (1) Assuming unused inputs are returned to voltage not greater than 4.0 Vdc.
- (2) The switching characteristics of the MTTL III family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turn-on delay and the turnoff delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2}$$
 ns

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative output transition from the 2.0 V to the 1.0 V level.

"NAND" GATES

The basic gate of the MTTL III logic family is the positive logic NAND gate. This gate is characterized by high speed, good load driving capability, superior transfer characteristic, and freedom from ringing problems. Representative of the various NAND gates presently available in the MTTL III family is the 4-input NAND gate (1/2 of the MC3010) shown in Figure 3,

"AND" GATES

While it is possible to design a complete logic system with NAND logic, it is often desirable to use other logic forms to save circuits, power dissipation, and propagation delay. Therefore, the positive logic AND function has been added to the MTTL III family.

Examples of the AND function are the standard quad 2-input gate, dual 4-input gate, dual 4-input power gate and a dual 3-input, 3-output line driver.

The technique used to form the AND function is the addition of an inverter to the basic NAND circuit. As shown in Figure 4. the inverter transistor with a collector resistor and an offset diode connected to its emitter is inserted between the multiple-emitter input transistor and the basic circuit phase-splitter transistor. The extra inversion adds only 3.0 ns propagation delay and about 6.0 mW additional power dissipation.

FIGURE 3 - MTTL III POSITIVE LOGIC "NAND" GATE CIRCUIT

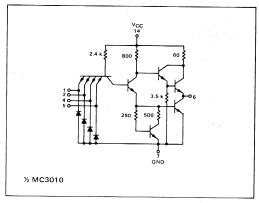
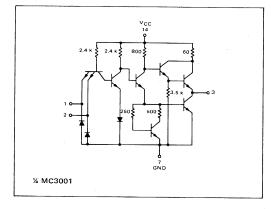


FIGURE 4 - MTTL III POSITIVE LOGIC "AND" GATE CIRCUIT





GENERAL INFORMATION SECTION

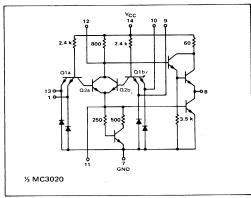
"AND-OR-INVERT" GATES

Unlike the MDTL family of logic circuits, the outputs of MTTL logic circuits cannot be tied together to perform the "Implied AND", often called the "Wired OR" function. If the outputs of the MTTL family devices are tied together, the lower output transistor of one circuit and the upper output transistor of another circuit can be "on" simultaneously. This condition provides a low-impedance path from VCC to ground, and due to excessive current flow, the saturated output state cannot be maintained and the desired logic function is not satisfied.

To retain the logical advantages offered by the "Implied AND" with the speed and load driving capability of an active pullup, the MTTL III family offers an AND-OR-INVERT Gate. The
gate in Figure 5 incorporates two 2-input AND function is provided
by two multiple-emitter input transistors (Q1a and Q1b). The OR
and INVERT operation is accomplished by two paralleled transistors (Q2a and Q2b) sharing a single collector resistor and a
single bypass network. These paralleled transistors in turn drive
the standard output.

The common collector and emitter nodes of one gate in each package are available externally to permit expansion.

FIGURE 5 - MTTL III "AND-OR-INVERT" GATE CIRCUIT



EXPANDER AND EXPANDER NODES

The ORing nodes of ½ the MC3020 dual AND-OR-INVERT Gate (Figure 5) are available for expanding the number of AND gates to four. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 1.0 ns/pF.

"NOR" GATES

To save inverters, the system designer often needs the positive logic NOR function as well as the negative logic NOR available with the standard NAND gate. This capability is incorporated in the MTTL III line in the form of the MC3002, quad 2-input NOR Gate. The NOR gate is a modified AND-OR-INVERT gate with only a single emitter on each input transistor, as shown in Figure 6.

"OR" GATES

To provide the system designer with still another tool for optimum design, the MTTL III Series also offers the positive logic OR function. As shown in Figure 7, the OR is essentially a NOR gate with an additional inverter.

POWER GATES

Standard MTTL III gates offer good load driving capability and high fan-out. In most systems, however, there are a few applications that exceed the capability of a standard gate. The MTTL III power gates, shown in Figure 8, are designed to meet these requirements with a minimum of additional circuitry. Available in both NAND and AND functions, the power gates feature output circuitry designed to provide twice the fan-out of conventional gates: 20 standard gate loads instead of 10.

FIGURE 6 – MTTL III POSITIVE LOGIC "NOR" GATE CIRCUIT

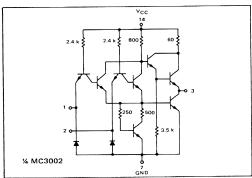
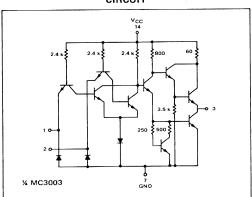


FIGURE 7 – MTTL III POSITIVE LOGIC "OR" GATE CIRCUIT



LINE DRIVERS

To minimize switching transients on long lines, the MTTL III family includes dual 3-input/3-output series-terminated line drivers. Two outputs have 75-ohm resistors in series with the standard output node, and one is connected directly to the node. A good match can be made at the output of each resistor when driving 93-ohm coax or 120-ohm twisted pair. For loads of 50 to 93 ohms, the two resistive outputs are paralleled for impedance matching. The non-resistive output can be used to drive adjacent loads in a normal fashion. The total number of output loads connected to the direct output (non-resistive output) is the standard fan-out of 10, minus the number of resistor terminated outputs being used.

Figure 9 shows 1/2 of the circuit of the MC3029, dual 3-input, 3-output series terminated NAND line driver. Figure 10 shows a typical application of this circuit and Figure 11 demonstrates the effects of series termination without a significant loss in high state noise immunity.

FIGURE 8 - MTTL III POWER GATE CIRCUIT (AND)

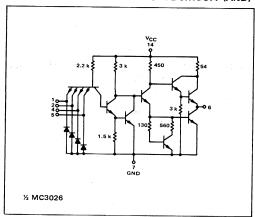
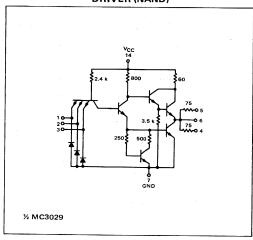


FIGURE 9 — MTTL III TERMINATED LINE DRIVER (NAND)



MTTL III

GENERAL INFORMATION SECTION

FIGURE 10 – TYPICAL APPLICATION OF THE LINE DRIVER

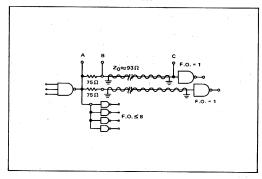
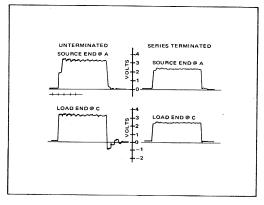


FIGURE 11 – EFFECTS OF SERIES TERMINATION WITH A MTTL III GATE DRIVING A 93-OHM LINE



OPERATING CHARACTERISTICS OF FLIP-FLOPS

The cornerstone of any modern logic family is the capability of its storage elements. The MTTL III flip-flops are designed to give maximum logic performance with fewer system restrictions than their predecessors. Three basic designs are typified by the MC3050, MC3060 and MC3061/MC3062. Common to all designs are:

1. Edge clocking.

The flip-flop is clocked at the normal MTTL III threshold voltage (approximately 1.5 V @ 25° C).

2. Overriding asynchronous inputs.

The direct SET and RESET inputs control the operation of the flip-flop regardless of the state of the clock or the information on synchronous inputs.

GENERAL INFORMATION SECTION

3. Short set-up times.

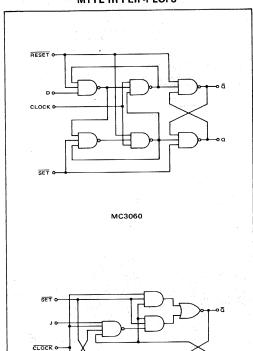
Prior to the clocking edge, the input information must become stable. The MTTL III flip-flops require only a minimum of time to read a "1" or a "0". Therefore data may be applied anytime in the clock period except during the time interval between the Set-up and Hold times. This characteristic permits higher clock frequencies or eliminates the necessity for critical control of clock pulse width.

 All inputs to the storage elements including the clock input have inputs that are compatible with all three MTTI families. The MC3050 and MC3060 flip-flops are positive edge triggered storage elements. That is, the inputs are enabled on the negative edge of the clock and the information is stored in the flip-flop on the positive edge of the clock. The MC3061 and MC3062 dual flip-flops are negative edge triggered devices and therefore operate in precisely the opposite manner. That is, data is stored on the negative edge of the clock.

In addition to the previously mentioned storage elements. The MC3052 Master-Slave flip-flop is also available. Data is stored in the Master flip-flop when the clock is low and transferred to the Slave flip-flop when the clock goes high.

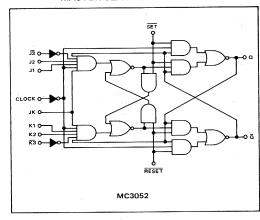
Detailed discussion of each of the MTTL III flip-flops is provided on the individual data sheets.

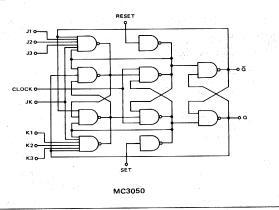
FIGURE 12 – LOGIC DIAGRAMS OF EDGE-CLOCKED MTTL III FLIP-FLOPS



MC3061

FIGURE 13 - LOGIC DIAGRAM OF MTTL III MASTER-SLAVE J-K FLIP-FLOP





GENERAL INFORMATION SECTION

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL circuit, the designer must always be aware of the problems caused by very high switching speeds. These switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the upper RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions will help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rates of change of current and voltage for a single MTTL III gate are in the range of $10^7 \, \text{A/s}$ and $108 \, \text{V/s}$ respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of $100 \, \text{mils}$ or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL III circuits. A comparatively large, low-inductance type capacitor (in the 1.0 µF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 µF capacitors for every five packages throughout a breadboard is adequate to suppress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The typical average dc power dissipation is given for each MTTL III device (3). It should be noted that the totem-pole output common to all high-level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.4 mW/MHz/output for a 15-pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL III circuits.

Unused Inputs and Unused Gates

To minimize potential problems resulting from external noise, the unused inputs of any MTTL III logic circuit should not be left open, but should either be tied to the used inputs or returned to a voltage between 2.0 and 5.5 Vdc. (For flip-flops, see appropriate data sheet for additional detail.) If the unused inputs are returned to a voltage, care should be exercised to insure that the absolute voltage between the most negative input level and that voltage does not exceed +5.5 volts. The total number of inputs that can be tied to the output of any driving gate is 25. (This is defined as high-state output loading factor.) It should be noted that the low-state output loading rules must still be maintained. The minimum logical "1" level for the high-state output loading is summarized for $V_{\rm CC} = 5.0$ V, $V_{\rm IL} = 1.1$ V, and $I_{\rm OH} = -2.0$ mA: $V_{\rm OH} = 2.5$ volts minimum @ 0°C.

To minimize power drain, the inputs of any unused gate in a package should be maintained at the level that would place the outputs in the high state (the low power dissipation state).

(3)
$$P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where IPDL and IPDH are the typical current drains at V_{CC} = +5.0 V.

MAXIMUM RATINGS

Value	Unit
+7.0	Vdc
4.5 to 5.5	Vdc
+5.5	Vdc
+5.5	Vdc
0 to +75	°C
-65 to +175	°C
	+7.0 4.5 to 5.5 +5.5 +5.5 0 to +75

MTTL III

GENERAL INFORMATION SECTION

DEFINITIONS

	DEFINITIONS	*Hold "0"
BVin	Input breakdown voltage	tHold "1"
CT	Total parasitic capacitance, which includes probe, wiring, and load capacitances	△tod
Mental C	Collector current	Authorization property
Ico	Expander collector leakage current	
In a	Input diode current with negative voltage applied	△t _{pd} /pF
restate to the conservation	Emitter current	and the self-time of the territory of
I _E O	Expander emitter leakage current	^t pd "0"
IEXE	Expander drive current at emitter node of AND-OR-INVERT gate	tpd "1"
1¢	Input forward current with V _{CC} applied	t _{sd} "0"
IF1	Input forward current with VCCL applied	ted "1"
IF2	Input forward current with VCCH applied	Set "0"
lFC.	Clock input forward current	"这种"的一种"一种"。
IFD	D input forward current	tSet "1"
IFJ	J input forward current	and the second of
lek .	K input forward current	TPin
¹ FJK	JK input forward current	TPout
- IFR	RESET input forward current	VBE max
IFS	SET input forward current	
distributed line and access	Input current	V _{BE min}
Imax	Maximum rated power supply current with V _{max} applied	Vcc
Юн	Output high state current	У ссн
IOHA	Unterminated output high state current	VCCL
онв. с	Terminated output high state current	Vo
loL	Output low state current	VEE1
OL1	Output low state current with VCCL applied	VEE2
OLIA	Unterminated output low state current with VCCL	
OLIA.	applied	VF
101.2	Output low state current with VCCH applied	Уін
IOL2A	Unterminated output low state current with VCCH applied	VIHX
OL1B.10	Terminated output low state current with VCCL	VIL.
OE IB. 10	applied	V _{max}
OL2A, 2C	Terminated output low state current with VCCH	Уон
OLZA,ZO	applied	YOL
more IPD	Flip-flop power supply drain current	VOL1
IPDH .	Power supply drain with inputs high	Vol.2
IPDL	Power supply drain with inputs low	VOL3
le le	Input leakage current	No.
IRC	Clock input leakage current	VOL4
IRD	D input leakage current	Ve
IRJ.	J input leakage current	VRH
IRK	K input leakage current	,,,,,

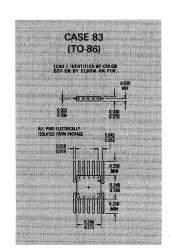
Short-circuit current Pulse used to set flip-flop state Pulse repetition frequency Pulse width Fall time Hold "0" Minimum time that low state data must be maintained after the clocking edge Hold "1" Minimum time that high state datamust be maintained after the clocking edge Average increase in propagation delay per expander AND gate when connected to an AND-OR-INVERT gete Topd/pF Increased propagation delay caused by additional capacitance at expansion points of "1" Turn-off delay Filse time Turn-off delay Filse time Turn-off delay from asynchronous input Minimum time that low state data must be applied prior to the clocking edge Pin Test point at input of device under test Emitter node threshold voltage for logic "0" output level MCC Power supply voltage Low power supply voltage Low power supply voltage Low power supply voltage Low power supply voltage (CCL High power supply voltage Voltage applied to expander emitter node for Ico test Waximum logic "0" level output voltage Maximum logic "0" level output voltage Output leigh voltage with Ico source current Voltage applied to expander emitter for Vol test Net max Maximum logic "0" level output voltage Output high voltage with Ico source current Voltage was pure to voltage on terminated output with VcCL applied Maximum output low voltage on terminated output with VcCL applied Maximum output low voltage on terminated output with VcCL applied Maximum output low voltage on terminated output with VcCL applied Maximum output low voltage on terminated output with VcCL applied More Maximum output low voltage on terminated output with VcCL applied More Maximum output low voltage on terminated output with VcCL applied More Maximum output low voltage on terminated output with VcCL applied	3R	RESET input leakage current
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VEE1 Voltage applied to expander emitter for V _{OL} test VEE2 Voltage applied to expander emitter node for I _{CO} test VF Maximum logic "0" level output voltage VIH Logic "1" threshold voltage VIHX Reduced supply voltage to hold input above threshold and to prevent noise from entering the device VIL Logic "0" threshold voltage VIL Logic "0" threshold voltage Maximum rated power supply voltage VOH Output high voltage with I _{OH} source current VOL Output low voltage with I _{OH} source current VOL1 Maximum output low voltage with V _{CCL} applied VOL2 Maximum output low voltage on terminated output with V _{CCL} applied VOL4 Maximum output low voltage on terminated output with V _{CCL} applied VOL4 Maximum output low voltage on terminated output with V _{CCL} applied VOL4 Maximum output low voltage on terminated output with V _{CCL} applied V _R Logic "1" minimum reverse voltage		Diode clamp voltage
VEE2 Voltage applied to expander emitter node for I _{CO} test VF Maximum logic "0" level output voltage VjH Logic "1" threshold voltage VjHX Reduced supply voltage to hold input above threshold and to prevent noise from entering the device VjL Logic "0" threshold voltage Vmax Maximum rated power supply voltage VOH Output high voltage with I _{OH} source current VoL Output low voltage with I _{OH} source current VoL1 Maximum output low voltage with V _{CCH} applied VoL2 Maximum output low voltage with V _{CCH} applied VoL3 Maximum output low voltage on terminated output with V _{CCH} applied VoL4 Maximum output low yoltage on terminated output with V _{CCH} applied VoL4 Maximum output low yoltage on terminated output with V _{CCH} applied Vg Logic "1" minimum reverse voltage		
ViH Logic "1" threshold voltage ViHX Reduced supply voltage to hold input above threshold and to prevent noise from entering the device ViL Logic "0" threshold voltage Vmax Maximum rated power supply voltage Output high voltage with IOH source current VoL Output low voltage with IOL source current VoL1 Maximum output low voltage with VCCH applied VoL2 Maximum output low voltage with VCCH applied VoL3 Maximum output low voltage on terminated output with VCCH applied VoL4 Maximum output low yoltage on terminated output with VCCH applied VoL4 Maximum output low yoltage on terminated output with VCCH applied Logic "1" minimum reverse voltage		Voltage applied to expander emitter node for ICO
VIH Logic "1" threshold voltage ViHX Reduced supply voltage to hold input above threshold and to prevent noise from entering the device ViL Logic "0" threshold voltage Vmax Maximum rated power supply voltage Output high voltage with IOH source current VoL Output low voltage with IOH source current VoL1 Maximum output low voltage with VCCH applied VoL2 Maximum output low voltage with VCCH applied VoL3 Maximum output low voltage on terminated output with VCCH applied VoL4 Maximum output low yoltage on terminated output with VCCH applied VoL4 Maximum output low yoltage on terminated output with VCCH applied Vol Maximum output low yoltage on terminated output with VCCH applied Vol Maximum output low yoltage on terminated output	Ve	
VIHX Reduced supply voltage to hold input above threshold and to prevent noise from entering the device V _{IL} Logic "0" threshold voltage V _{max} Maximum rated power supply voltage VOH Output high voltage with IOH source current V _{OL} Output low voltage with IOH source current V _{OL1} Maximum output low voltage with V _{CCL} applied V _{OL2} Maximum output low voltage with V _{CCL} applied V _{OL3} Maximum output low voltage on terminated output with V _{CCL} applied V _{OL4} Maximum output low voltage on terminated output with V _{CCL} applied V _{OL4} Maximum output low voltage on terminated output with V _{CCL} applied V _{OL5} V _{OL6} V _{OL7} V		
Vmax Vmax Vol. Output high voltage with IOH source current Vol. Output low voltage with IOH source current Vol.1 Maximum output low voltage with VCCL applied Vol.2 Maximum output low voltage with VCCH applied Vol.3 Maximum output low voltage with VCCH applied Vol.4 Maximum output low voltage on terminated output with VCCL applied Vol.4 Maximum output low voltage on terminated output with VCCH applied Vol.4 Logic "1" minimum reverse voltage		
Vmax Maximum rated power supply voltage VoH Output high voltage with IOH source current VoL Output low voltage with IOL source current VoL1 Maximum output low voltage with VCCL applied VoL2 Maximum output low voltage with VCCH applied VoL3 Maximum output low voltage on terminated output with VCCL applied VoL4 Maximum output low voltage on terminated output with VCCH applied Voltage voltage on terminated output voltage voltage voltage Voltage voltage voltage	VIL	Logic "0" threshold voltage
VOH Output high voltage with IOH source current VOL Output low voltage with IOH source current VOL1 Maximum output low voltage with VCCL applied VOL2 Maximum output low voltage with VCCH applied VOL3 Maximum output low voltage on terminated output with VCCL applied VOL4 Maximum output low voltage on terminated output with VCCH applied VOL4 Logic "1" minimum reverse voltage		Maximum rated power supply voltage
Vol.1 Output low voltage with I _{O1} source current Vol.1 Maximum output low voltage with V _{CCL} applied Vol.2 Maximum output low voltage with V _{CCL} applied Vol.3 Maximum output low voltage on terminated output with V _{CCL} applied Vol.4 Maximum output low voltage on terminated output with V _{CCL} applied V _R Logic "1" minimum reverse voltage		Output high voltage with IOH source current
VOL1 Maximum output low voltage with V _{CCL} applied V _{OL2} Maximum output low voltage with V _{CCL} applied V _{OL3} Maximum output low voltage on terminated output with V _{CCL} applied V _{OL4} Maximum output low voltage on terminated output with V _{CCL} applied V _{OL5}		
VOL2 Maximum output low voltage with V _{CCH} applied VoL3 Maximum output low voltage on terminated output with V _{CCL} applied Maximum output low voltage on terminated output with V _{CCH} applied V _R Logic "1" minimum reverse voltage		
VOL3 Maximum output low voltage on terminated output with V _{OL} applied V _{OL} Maximum output low voltage on terminated output with V _{OL} applied V _R Logic "1" minimum reverse voltage		
VOL4 Maximum output low voltage on terminated output with VCCH applied VR Logic "1" minimum reverse voltage		Maximum output low voltage on terminated output
V _R Logic "1" minimum reverse voltage	VOL4	Maximum output low voltage on terminated output
	VB	

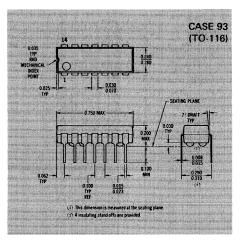
JK input leakage current

IAJK

PACKAGING

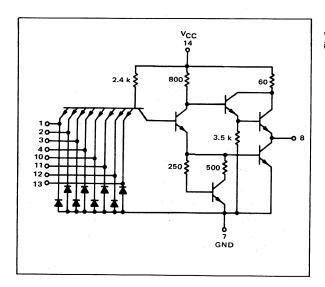
All MTTL III integrated circuits are available in the TO-85 14 lead flat package and TO-116 dual in-line plastic package. Suffix "F" to the basic type number; to order plastic package, add Suffix "P".



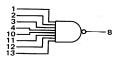


MTTL III MC3000 series

MC3015



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders and decoders.



Positive Logic:

8 = 1 • 2 • 3 • 4 • 10 • 11 • 12 • 13

Negative Logic:

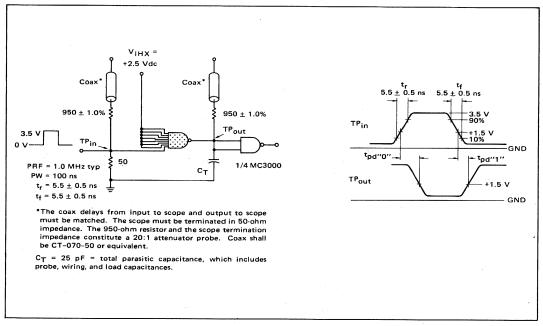
8 = 1 + 2 + 3 + 4 + 10 + 11 + 12 + 13

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 22 mW typ/pkg Propagation Delay Time = 8.0 ns typ

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one input of this device. To complete testing, sequence through remaining inputs in the same manner.



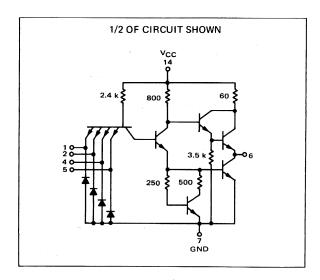
@Test	
Temperature	•
0°0	

ſ					-		TEST	CURR	ENT/VOLT	AGE VALUES	\$				
,			mA							١	olts .				
ture	lou	I _{OL2}	Іон	l _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}	V _{IHX}
o°c	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-
5°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
5°c l	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-

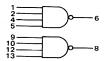
		Pin				est Limi			,					TEST	CURR	ENT /	VOLTA	GE APPLIED	TO PINS LI	STED BEL	OW:				
		Under	0	°C	+2	5°C	+7.	5°C				Γ.	Τ.	Γ.		Γ.,			.,		Τ.,			. v	
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	OL1	I _{OL2}	l _{ОН}	lin	1 _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2, 3, 4, 10, 11, 12, 13	-	-	14		-	7
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	- 1	-	2, 3, 4, 10, 11, 12, 13	-	- '		14	-	7
Leakage Current	IR	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 3, 4, 7, 10, 11, 12, 13
Breakdown Voltage	BVin	1	-	-	5.5	-	-	-	Vdc	-	-	-	1			-	-	-		-	-	-	14	-	2, 3, 4, 7, 10, 11, 12, 13
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-,	14	-	-	7
Output Output Voltage	V _{OL 1}	8	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	1	-	-	2, 3, 4, 10 11, 12, 13	-	-	14	-	-	7
	V _{OL 2}	8	-	0.4	-	0.4	-	0.4	Vdc	-	8	-	-	-	-	1	-	-	2, 3, 4, 10 11, 12, 13	-	-	-	14	-	7
	v _{он}	8	2.5	-	2.5	-	2.5	-	Vdc	-	-	8	-	-	1	-	-	-	2, 3, 4, 10, 11, 12, 13	-	-	14	-	-	7
Short-Circuit Current	I _{SC}	8	-	-	-30	-100	-	-	mAdc	- ,	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 4, 7,8, 10, 11, 12,13
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	6.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13
Power Supply Drain	I _{PDH}	14	1 -	9.0	-	9.0	-	9.0	mAdc		-	-	-	-	-	-	-	-	1, 2, 3, 4, 10, 11, 12, 13	-	14	-	-	-	7
	IPDL	14	-	4.3	-	4.3		4.3	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13
Switching Parameters										Pulse In	Pulse Out									1				2, 3, 4, 10,	
Turn-On Delay	t _{pd''0''}	1, 8	-	-	-	12		-	ns	1	8	_	-	_	-	-	-	-	-	-	14			11, 12, 13	
Turn-Off Delay	tpd"1"	1, 8	-	-	-	12	-	-	ns	1	8	-	-	-	-	-	-	- 1:	-	-	14	-	-	2, 3, 4, 10 11, 12, 13	7

MTTL III MC3000 series

MC3010



This device consists of two 4-input NAND gates. These gates may be cross-coupled to form a set-reset flip-flop.



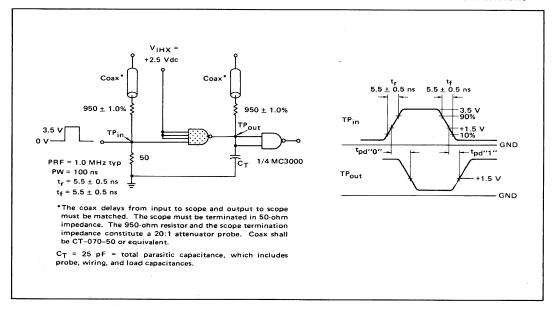
Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$ Negative Logic: 6 = 1 + 2 + 4 + 5

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 44 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



							TEST	CURR	ENT/VOLT	AGE VALUES	;		-		
@Test		r	nA							٧	olts				
Temperature	l _{ol1}	I _{OL2}	IOH	l _{in}	ID	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	Vccr	V _{cch}	V _{IHX}
0°C	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5. 0	4.5	5. 5	-
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5. 5	-

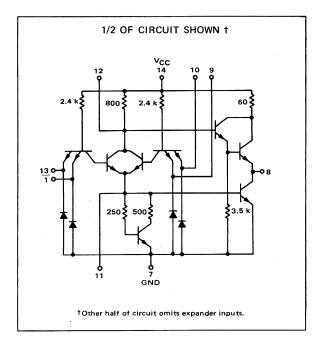
		Pin		M	3010	Test Lin	nits							TEST	CURE	RENT /	VOLTA	GE APPLIE	D TO PINS LI	STED REI	OW.	-	<u> </u>		1
		Under	0°C		+25°C		+7	5°C		 	Т	1			·	·		Т	10 11113 21				,		4
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	loli	I _{OL2}	Юн	lin	I _D	VIL	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	Vccr	V _{cch}	V _{IHX}	Gnd
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	14	-	-	7*
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAde	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 4, 5, 7 *
Breakdown Voltage	BV _{in}	1	-	-	5.5	-	-	-	Vdc	-	-		1	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7 *
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	† -	-	-	-	-	14	-	-	7
Output Output Voltage	V _{OL 1}	6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	-	1	-	-	2, 4, 5	-	-	14	-	-	7*
	V _{OL 2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	6	-	-	-	-	1	-	-	2, 4, 5	-	-	-	14	-	7*
	v _{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	6	-	-	1	-	-	-	2, 4, 5	-	-	14	-	-	7*
Short-Circuit Current	I _{SC}	6	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,4,5,6,7*
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	12.5	-	-	mAde	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	18	-	18	-	18	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7
	I _{PDL}	14	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters Turn-On Delay	t	1, 6				10			ns	Pulse In	Pulse Out	_		_		_		_	_	_	14	_	_	2, 4, 5	7*
Turn-Off Delay	tpd"0	1, 6	 - -	<u> </u>	ļ- <u>-</u>	10	-	-		1	6	<u> </u>	Ŀ			-	ļ <u>. </u>	-	ļ- <u>-</u>	<u> </u>	14	-	_	2, 4, 5	7*
rum-On Detay	^t pd''1''	1,0	1 -	1 -	1 -	1 10	-	-	ns	١ '	0	-	1 -		I -	1 -	-	1 -	1 -	-	1 17	1	-	2, 2, 3	1 '

^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

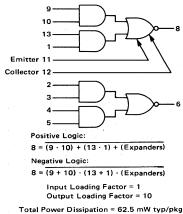
EXPANDABLE DUAL 2-WIDE 2-INPUT "AND-OR-INVERT" GATE

MTTL III MC3000 series

MC3020



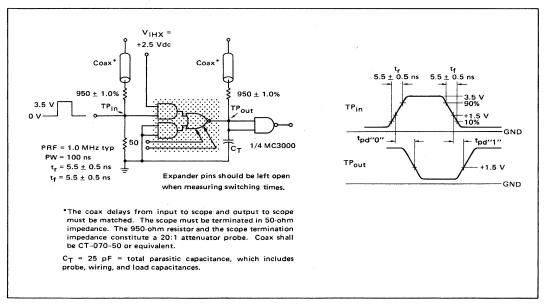
One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together, driving an output inverter, and the ORing nodes are available for expansion. Up to four AND gates can be ORed together using the MC3030 expander. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Total Power Dissipation = 62.5 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

ı	TEST CURRENT/VOLTAGE VALUES																					
@Test				mΑ				Volts														
Temperature	l _{OL 1}	I _{OL 2}	I _{OH}	l _{in}	I _D	l _E	IEXE	VIL	V _{IH}	V _F	V_R	V _{RH}	A ^{max}	V _{cc}	٧ _{ccι}	V _{CCH}	V _{IHX}					
0°C	19	23	-2.0	-	-	0.3	0.50	1.1	2.0	0.4	2.5	4.0	-	5. 0	4.5	5. 5	-					
+25°C	19	23	-2.0	1.0	-10	0, 3	0, 55	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5					
+75°C	19	23	-2.0	-	-	0.3	0.70	0.9	1.8	0.4	2.5	4.0	<u> </u>	5.0	4.5	5.5						

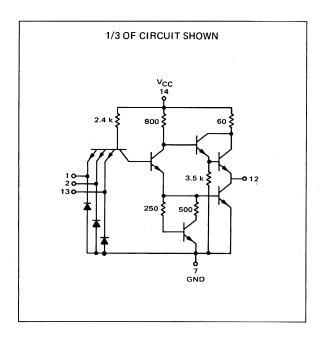
		Pin				0 Test I			,						TEST	CURREN	T / VO	LTAGE	APPLIE	D TO PINS	LISTED BELO)W:							
el		Under	0°		+2		+7 Min	5°C Max	Unit	1	l _{OL 2}	I _{OH}	ī	I _D	l _E	IEXE	٧٫١	VIH	٧ _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{ccl}	V _{CCH}	V _{IHX}	Gnd		
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	max	Unit	OL 1	*OL 2	-ОН	¹in	U.D	- E	EXE	- 11.	III.			, KA								
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAde	-	-	-	-	-	-	-	-	-	1	-	13	-	-	14	-	-	7,9,10*		
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAde	-	-	-	-	-	-	-	-	-	1	-	13	-	-	-	14	-	7, 9, 10*		
Leakage Current	IR	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	-	-	1	-	-	-		14	-	7, 9, 10, 13*		
Breakdown Voltage	BV _{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	14	-	7, 9, 10, 13 *		
Clamp Voltage	v _D	1	-	-		-1.5	-	-	Vdc	-	-	-	-	1			-	-	-	-	-	-	-	14	-	-	7, 9, 10 *		
Output Output Voltage	V _{OL1}	8 8	-	0. 4 0. 4	-	0.4 0.4	-	0. 4 0. 4	Vdc Vdc	8 8	-	-	-	-	-	11, 12	-	1 -	-	-	13	-	-	14 14	:	-	7, 9, 10 * 1,7,9,10,13		
	V _{OL 2} V _{OL 2}	8 8	-	0.4 0.4	-	0, 4 0, 4	-	0.4	Vdc Vdc	-	8	-	-	-	-	11, 12	-	- 1	-	-	13	-	-	-	14 14	-	1,7,9,10,13* 7,9,10*		
	v _{OH}	8	2.5	-	2.5	-	2.5	-	Vdc	-	-	8	-	-	-	-	1	-	-	-	13	-	Ŀ	14	-	-	1, 7, 10 *		
Short-Circuit Current	ISC	8	-	-	-30	-100	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 7, 8, 9, 10, 13 *		
Base- Emitter Voltage	v _{BE max}	- 11	-	1.010	-	0.975	-	0.935	Vdc	8	-	-	-	-	-	11, 12	-		-	-	-	-	-	14	-	-	1, 9, 10,		
	V _{BE min}	11	0,70	-	0.65	-	0.55	-	Vdc	-	-	-	-	-	11	-	-	-	-	-	-	-	-	14	-	-	1, 9, 10, 12,13 *		
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	24	-	-	mAde	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7, 9,10,13		
Power Supply Drain	I _{PDH}	14	-	22	-	22	-	22	mAdc	-	-	-	-	-	-		-	-	-	-	1, 2, 3, 4, 5, 9, 10, 13	-	14	-	-	-	7		
	IPDL	14	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	-	Ι-	-	-	-	14	-	-	-	1,2,3,4,5,7, 9,10,13		
Switching Parameters										Pulse In	Pulse Out												14			13	7,9,10*		
Turn-On Delay	t pd''0''	1, 8		-	-	12	-	-	ns	1	8		-	-	-	-	_	Ŀ	ļ	-			14	ļ	<u> </u>				
Turn-Off Delay	tpd"1"	1, 8	-	-	-	12	-	-	ns	1	. 8	-	-	-	-	-	-	-	-	-	-	-	14	-		13	7, 9, 10 *		

^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

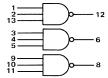
TRIPLE 3-INPUT "NAND" GATE

MTTL III MC3000 series

MC3005



This package consists of three 3-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



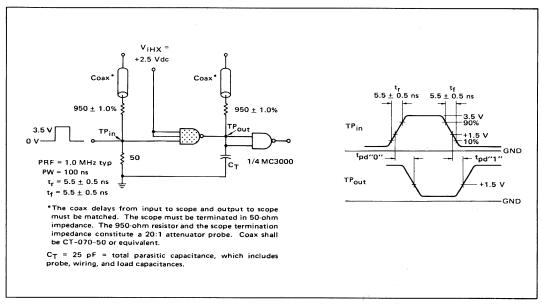
Positive Logic: $12 = \overline{1 \cdot 2 \cdot 13}$ Negative Logic: $12 = \overline{1 + 2 + 13}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 66 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one 13 gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through religious



							TEST	CURR	ENT/VOLT	AGE VALUE	5				
@Test		r	nA	,						٧	olts				
Temperature	l _{OL1}	I _{OL2}	loh	l _{in}	l _D	٧ _{IL}	VIH	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{cch}	V _{IHX}
0°C [19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5. 0	4.5	5. 5	_
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	—	5. 0	4.5	5. 5	

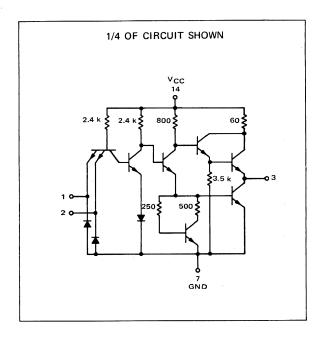
		Pin		MC	3005	Test Lim	its							TEST	CHE	PENT /	VOLTA	GE ADDITE	D TO PINS L	CTED DE	5.0	4.5	5.5	-	┪
		Under	0	°C	+2	5°C	+7	′5°C	Ì	 			т	1.5	COM	LIVI /	VOLIA	OL AFFLIE	D IO PINS L	SIED BEL	.UW:				
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	lou	l _{OL2}	Іон	l _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{cc} ι	V _{CCH}	VIHX	Gnd
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	m Adc	-	-	-	-	-	-	-	1	-	2, 13	-	-	14	-	-	7*
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAde	-	-	-	-	-	-	-	1	-	2, 13	-		-	14	-	7*
Leakage Current	I _R	1	-	80	-	80	-	80	μAde	-	-	-	-	-	-	-	-	1	 -	-	-	-	14	-	2, 7, 13*
Breakdown Voltage	BV _{in}	1	-	-	5. 5	-	-	-	Vdc	-	-	-	1	-	-	-	-		-	-	-	-	14		2, 7, 13 *
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-		-	-	14	-	-	7*
Output Output Voltage	V _{OL 1}	12	-	0.4	-	0.4	-	0.4	Vdc	12	-	-	-	-	-	1	-	-	2, 13	-	-	14	-		7*
	V _{OL 2}	12	-	0.4	-	0.4	-	0.4	Vdc	-	12	-	-	-	-	1	-	-	2, 13	-	-		14	-	7*
	v _{он}	12	2.5	-	2.5	-	2.5	-	Vdc	-	-	12	-	-	1	-	-	-	2, 13	-	-	14	-	-	7*
Short-Circuit Current	I _{SC}	12	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-		14	-	-		1, 2, 7,* 12, 13
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	20	-	-	mAde	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7, 9, 10, 11, 13
Power Supply Drain	I _{PDH}	14	-	27	-	27	-	27	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 11, 13	-	14	-	-	-	7
	I _{PDL}	14	-	12.5	-	12.5	-	12.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,3,4,5,7, 9,10,11,13
Switching Parameters										Pulse In	Pulse Out														0,10,11,13
Turn-On Delay	^t pd''0''	1, 12	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-	-	-	14	-		2, 13	7*
Turn-Off Delay	t _{pd"1"}	1, 12	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-	-		14	-	-	2, 13	7*

^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

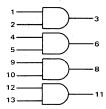
QUAD 2-INPUT "AND" GATE

MTTL III MC3000 series

MC3001



This device consists of four 2-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

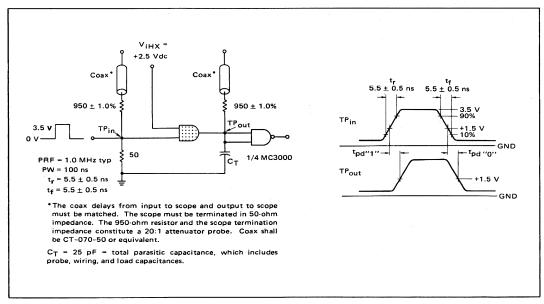


Positive Logic: $3 = 1 \cdot 2$ Negative Logic: 3 = 1 + 2

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 112 mW typ/pkg Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT



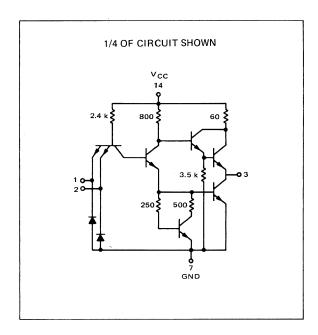
ELECTRICAL CHARACTERISTICS TEST CURRENT/VOLTAGE VALUES Volts Test procedures are shown for only one mΑ @Test gate. The other gates are tested in the same V_{IH} $V_{\rm max}$ V_{cc} V_{CCH} V_{IHX} V_{RH} V_{CCL} ΙD l_{OL2} Temperature OLI ГОН manner. Further, test procedures are shown 9for only one input of the gate under test. 10-5.0 4.5 5. 5 0°C 19 23 -2.0 1.1 2.0 0.4 2.5 4.0 To complete testing, sequence through re- 12-+25°C 19 23 -2.0 1.0 -10 1.1 1.8 0.4 2.5 4.0 7.0 5.0 4.5 5. 5 2.5 maining inputs. 5.0 4.5 5.5 +75°C 19 23 -2.0 0.9 1.8 4.0 -0.4 2.5 MC3001 Test Limits TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: Pin 0°C +25°C +75°C Under V_{max} V_{CCL} V_{IHX} I_D V_{IH} ٧_F V_{RH} V_{cc} V_{CCH} I_{OL2} lou lон Gnd Characteristic Symbol Test Min Max Min Max Min Max Unit Input 7 2* 1 Forward Current 1 -1.9 -1.9 -1.9 mAdc I_{F1} 14 7 1 2* -2.3 -2.3 -2.3 mAdc 1 I_{F2} 2,7 14 1 Leakage Current IR 1 80 80 80 μAdc 2,7 14 Breakdown Voltage BVin 5.5 Vdc 1 7 14 Clamp Voltage $v_{_{\rm D}}$ 1 -1.5 Vdc Output 7 2 * 14 Output Voltage $v_{\text{OL 1}}$ 3 0.4 0.4 0.4 Vdc 1 7 2* 14 V_{OL 2} 3 0.4 0.4 0.4 -Vdc 3 7 2 * 14 v_{OH} 3 2.5 2.5 2.5 3 _ -Vdc 3,7 1,2* 14 Short-Circuit 3 -30 -100 mAdc Current **Power Requirements** (Total Device) 7 1,2,4,5,9, 10,12,13 14 Maximum Power 14 34 mAdc I_{max} Supply Current 1,2,4,5,9, 14 Power Supply Drain mAde 14 24 24 24 I_{PDH} 10,12,13 1,2,4,5,7, 14 14 48 48 48 mAdc PDL 9,10,12,13 Switching Pulse Pulse Out Parameters 2 7 1 3 14 Turn-On Delay 1, 3 12 t_{pd''0''} ns7 14 2 Turn-Off Delay 1, 3 1 3

^{*}Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to \mathbf{V}_{BH} .

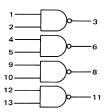
QUAD 2-INPUT "NAND" GATE

MTTL III MC3000 series

MC3000



This device consists of four 2-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.

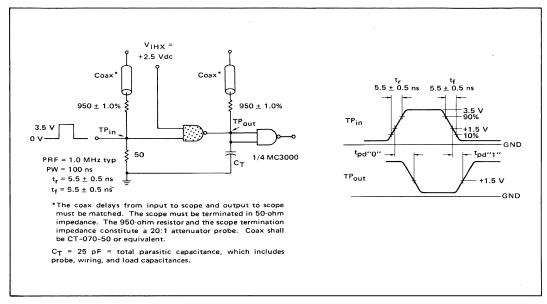


Positive Logic: $3 = \overline{1 \cdot 2}$ Negative Logic: $3 = \overline{1 + 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 88 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT



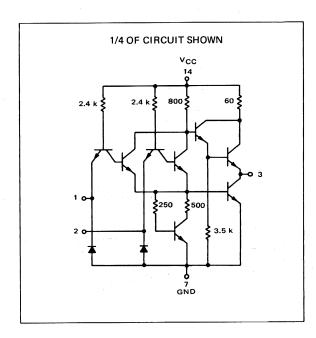
ELECTRICAL CHARACTERISTICS TEST CURRENT / VOLTAGE VALUES Test procedures are shown for only one mΑ Volts @Test gate. The other gates are tested in the same V_{IH} VRH ΙD V_{max} V_{cc} Vccr V_{IHX} lou I_{OL2} loh V_{CCH} Temperature manner, Further, test procedures are shown for only one input of the gate under test. 10-0°C 19 23 -2.0 1.1 2.0 0.4 2.5 4.0 5.0 4.5 5.5 To complete testing, sequence through re- 12-+25°C 19 23 -2.0 1.0 -10 1.1 1.8 0.4 2.5 4.0 7.0 5.0 4.5 5.5 2.5 maining inputs. +75°C 19 23 -2.0 0.9 1.8 0.4 2.5 4.0 5.0 4.5 5.5 MC3000 Test Limits TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: Pin 0°C +25°C +75°C Under V_{IL} V_{IH} V_{RH} V_{cc} V_{CCL} V_{IHX} Min Max Min Max Min Max Unit loli lol2 I_{OH} ΙD V_{CCH} Characteristic Symbol Test Gnd Input Forward Current 1 -1.9 -1.9 -1.9 mAdc 2 14 I_{F1} 1 -2.3 -2.3 -2.3 mAdc 1 2 14 I_{F2} Leakage Current 1 80 80 2,7 * 80 14 µ Adc Breakdown Voltage BV_{in} 1 5.5 -Vdc 1 -14 2,7* Clamp Voltage 1 -1.5 Vdc 1 14 7 * Output Output Voltage 3 VOL 1 0.4 0.4 0.4 Vdc 3 2 14 7* V_{OL 2} 3 0.4 0.4 2 7* 0.4 Vdc 3 1 -14 v_{OH} 3 2.5 -2.5 2.5 Vdc 3 1 2 14 7 * Short-Circuit I_{SC} 3 -30 -100 mAde 14 1, 2, 3, 7 * Current Power Requirements (Total Device) Maximum Power I_{max} 14 25 mAdc 14 1, 2, 4, 5, 7, Supply Current 9, 10, 12, 13 Power Supply Drain 14 36 1, 2, 4, 5, 9, 10, 12, 13 7 IPDH 36 36 mAdc 14 I_{PDL} 14 17.5 17.5 17.5 14 1, 2, 4, 5, 7, 9, 10, 12, 13 mAde Switching Pulse Pulse Parameters Out Turn-On Delay 1,3 3 14 2 7 * "0"bq 10 ns Turn-Off Delay 1,3 10 t_{pd"1"} ns 1 3 14 2 7*

^{*} Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

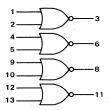
QUAD 2-INPUT "NOR" GATE

MTTL III MC3000 series

MC3002



This device consists of four 2-input NOR gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.

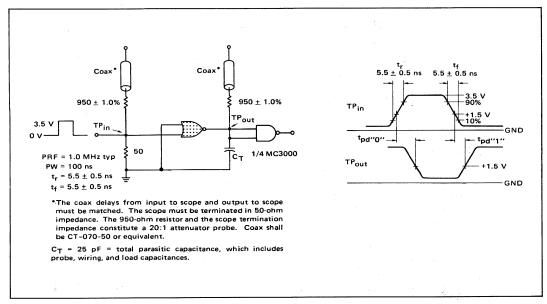


Positive Logic: $3 = \overline{1+2}$ Negative Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 122 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown only one input of the gate under test. 10—To complete testing, sequence through relationship inputs.



							TEST	CURRE	NT/VOLTA	GE VALUES				
@Test		ı	nA								/olts			
Temperature	I _{OL1}	I _{OL2}	Іон	l _{in}	ID	VIL	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{ccι}	V _{CCH}
o°c [19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5. 0	4.5	5. 5
+25°C [19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5
+75°C [19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	T -	5.0	4.5	5. 5

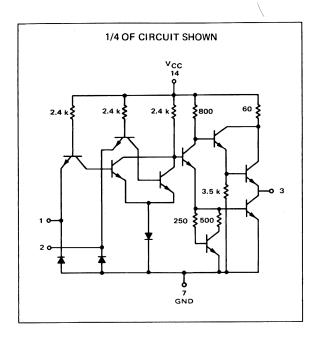
		Pin		MC	3002 1	est Lim	its							TEST	T CURR	ENT /	VOLTA	GE APPLIE	D TO PINS LI	STED BEL	OW:			
		Under	0	°C	+2	5°C	+7	5°C			T	1	Τ					Τ					r	
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	loli	I _{OL2}	Іон	lin	l _D	VIL	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{ccı}	V _{CCH}	Gnd
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	m Adc	-	-	-	-	-	-	-	1	-	2	-	-	14	-	7*
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAde	-	-	-	-	-	-	-	1	-	2	-	-	-	14	7*
Leakage Current	I_R	1	-	80	-	80	-	80	μAde	-	-	-	-	-	-	-	-	1	-	-	-	-	14	2,7*
Breakdown Voltage	BVin	. 1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	† - -	-	14	2,7*
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	†	14	-	7 *
Output Output Voltage	v _{OL1}	3		0.4	-	0, 4	-	0.4	Vdc	3	-	-	-	-	-	1	-	-	-	-	-	14	-	2, 7 *
	V _{OL 2}	3	-	0.4	-	0.4	-	0.4	Vdc	-	3	-	-	-	-	1	-	-	-	-	-	-	14	2, 7 *
	v _{OH}	3	2.5	-	2.5	-	2.5	-	Vdc	-	-	3	-	-	1	-	-	-	-	-	-	14	-	2, 7 *
Short-Circuit Current	ISC	3	-	-	-30	-100	-	-	mAde	-	-	-	-	-	-	-	-	-	-	-	14	-	-	1, 2, 3, 7 *
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	38	-	-	mAde	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I _{PDH}	14	-	43	-	43	-	43	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	7
	I _{PDL}	14	-	27	-	27	-	27	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters			-							Pulse In	Pulse Out							-						
Turn-On Delay	t _{pd''0''}	1, 3	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	-	14	-	-	2,7*
Turn-Off Delay	t pd''1''	1, 3	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	-	14	-	-	2, 7 *

^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

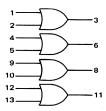
QUAD 2-INPUT "OR" GATE

MTTL III MC3000 series

MC3003



This device consists of four 2-input OR gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

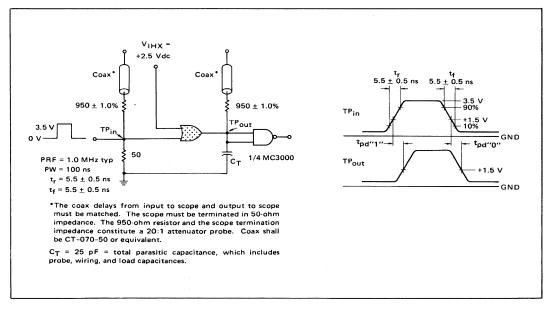


Positive Logic: 3 = 1 + 2Negative Logic: $3 = 1 \cdot 2$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in the same 5—manner. Further, test procedures are shown 9—for only one input of the gate under test. 10—To complete testing, sequence through re- 12—maining inputs. 13—



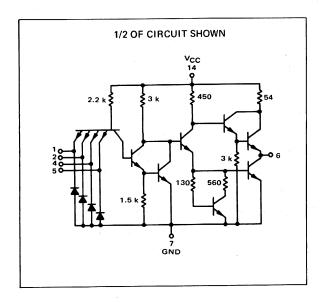
							TES	T CURI	RENT/VOLT	AGE VALUE	:S				
@Test		r	nΑ							٧	'olts				
Temperature	l _{ol1}	I _{OL2}	Іон	l _{in}	I _D	٧ _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	ν _{cc}	V _{ccι}	V _{CCH}	V _{IHX}
0°C	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5. 0	4.5	5. 5	-
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	I -	5.0	4.5	5. 5	-

		Pin				Test Lim					•	•		TEST	CURR	RENT / Y	VOLTA	GE APPLIE	TO PINS LI	STED BEL	OW:		<u> </u>		1
Characteristic	Svmbol	Under Test	Min	°C Max	+2 Min	5°C Max	+7 Min	5°C Max	Unit	lou	I _{OL2}	Гон	lin	I _D	V _{IL}	V _{IH}	VE	V _R	V _{RH}	V _{max}	V _{cc}	V _{ccl}	V _{cch}	V _{IHX}	Gnd
	37111001	1031	1400	IVIUX	JANIII.	Max	141111	71107	01111		012	0	1			_ in		<u> </u>	Kn .	max	1 00	cci	CCH	IIIA	
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2 *	-	-	14	-	-	7
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	- \	-	-	1	-	2 *	-	-	-	14	-	7
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1		-	-	-	14	-	2,7
Breakdown Voltage	BVin	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-		-	-	-	14	-	2,7
Clamp Voltage	v_{D}	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
Output Output Voltage	v _{OL1}	3	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	1	-	-	-	2*	-	-	14	-	-	7
	v _{OL2}	3	-	0.4	-	0.4	-	0.4	Vdc	-	3	-	-	-	1	-	-	-	2*	-	-	-	14	-	7
	v _{OH}	3	2.5	-	2.5	-	2.5	-	Vdc	-	-	3	-	-	-	1	-		2 *	-	-	14	-	-	7
Short-Circuit Current	ISC	3	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	1, 2 *	-	14	-	-	-	3,7
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	45	-	-	mAdc	-	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	14	-	-	-	-	7
Power Supply Drain	I _{PDH}	14	-	32	-	32	-	32	mAdc	-	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	-	14	-	-	-	7
	IPDL	14	-	55	-	55	-	55	m Adc	-	-	-	-	-	, -	-	-	-	-	-	14	-	-	-	1,2,4,5,7, 9,10,12,13
Switching Parameters										Pulse In	Pulse Out														
Turn-On Delay	t _{pd"0"}	1, 3	-	-	-	12	-	-	ns	1	3	-	-	-	-	-	-	-	•	-	14	-	-	2	7
Turn-Off Delay	t pd''1''	1, 3	-	-	-	12	-	-	ns	1	3	-	-	-	-	-	-	-	*	-	14	-	-	2	7

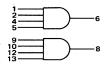
^{*}Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to $\rm V_{RH}$

MTTL III MC3000 series

MC3026



This device consists of two 4-input AND power gates. Each gate is designed for driving high fan-out loads (20).

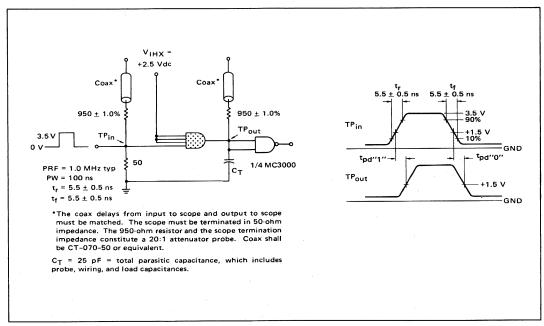


Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$ Negative Logic: 6 = 1 + 2 + 4 + 5

Input Loading Factor = 1.1
Output Loading Factor = 20

Total Power Dissipation = 90 mW typ/pkg Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



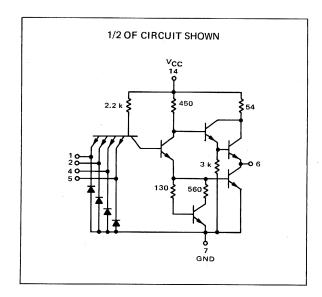
							TEST	CURR	ENT/VOLTA	AGE VALUES					
@Test		r	nA							V	olts				
Temperature	lou	I _{OL2}	Іон	lin	ID	V _{IL}	V _{IH}	٧ _F	V_R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}	V _{IHX}
0°C	38	46	-4.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5. 0	4.5	5. 5	-
+25°C	38	46	-4.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	38	46	-4.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5. 5	-

		Pin		MC	3026	Test Lim	its							TEST	T CURF	RENT /	VOLTA	GE APPLIEI	TO PINS LI	STED BEL	OW:				
		Under	0	°C	+2	5°C	+7	5°C		 -			Т.	т	Т	T	т	Т			Ι	Т			
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	l _{OL1}	I _{OL2}	Іон	lin	I _D	VIL	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _{F 1}	1	-	-2.1	-	-2.1	-	-2. 1	mAdc	-	-	-	-	-	-	-	1	-	2,4,5*	-	-	14	-	-	7
	I _{F 2}	1	-	-2.6	-	-2.6	-	-2.6	mAdc	-	T -	-	-	-	-	-	1	-	2, 4, 5 *	-	-	-	14	-	7
Leakage Current	I _R	1	-	80	-	80	-	80	μAde	-	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2, 4, 5, 7
Breakdown Voltage	BVin	1	-		5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2, 4, 5, 7
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	r	-	-	-	-	*	-	-	14	-	-	7
Output Output Voltage	V _{OL 1}	6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	1	-	-	-	2, 4, 5 *	-	-	14	-	-	7
	V _{OL 2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	6	-	-	-	1	-	-	-	2, 4, 5 *	-	-	-	14	-	7
	v _{OH}	6	2.5	T -	2.5	-	2.5	-	Vdc	-	-	6		-	-	1	-	-	2, 4, 5 *	-	-	14	-	-	7
Short-Circuit Current	I _{SC}	6	-	-	-50	-125	-	-	mAdc	-	7	-	-	-	-	-	-	-	1, 2, 4, 5 *	-	14	-	-	-	6, 7
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	22	-	-	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	14	-	-	-	-	7
Power Supply Drain	I _{PDH}	14	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	•	7
	I _{PDL}	14	-	38	-	38	-	38	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9,10,12,13
Switching Parameters	-									Pulse In	Pulse Out														
Turn-On Delay	^t pd''0''	1, 6	-	_	-	15	-	-	ns	1	6	-	_	-	_	-	_	-	*	-	14	-	-	2, 4, 5	7
Turn-Off Delay	t _{pd''1''}	1,6		-	-	15	-	-	ns	1	6	-	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	7

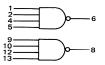
^{*} Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to \boldsymbol{v}_{RH} .

MTTL III MC3000 series

MC3025



This device consists of two 4-input NAND power gate circuits. Each gate is designed for driving high fan-out loads (20).

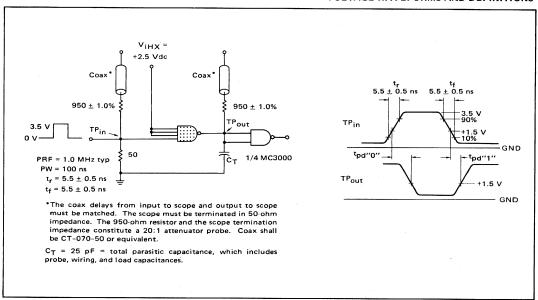


Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$ Negative Logic: 6 = 1 + 2 + 4 + 5

Input Loading Factor = 1.1
Output Loading Factor = 20

Total Power Dissipation = 70 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



1							TEST	CURR	ENT/VOLT	AGE VALUES					
@Test		n	nA							V	olts				
Temperature	l _{ol1}	I _{OL2}	Гон	lin	I _D	٧	VIH	V _F	V _R	V _{RH}	V _{max}	V _{cc}	۷ _{ccr}	V _{ccн}	V _{IHX}
o°c	38	46	-4.0	-	-	1.1	2.0	0.4	2.5	4. 0	-	5. 0	4.5	5. 5	-
+25°C	38	46	-4. Q	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	38	46	-4.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5. 5	_

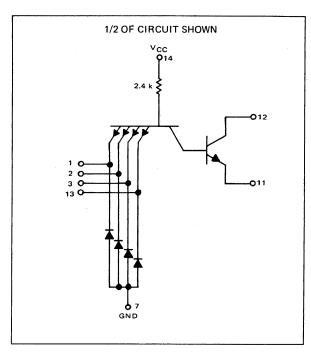
		Pin			3025 1	Test Lim	its							TES	CURR	ENT /	VOLTA	GE APPLIE	TO PINS LI	STED BEL	OW:				
		Under	0	°C	+2	:5°C		5°C			Γ.	г. —	Τ.		T	.,	\	٠,,	T ,,		T.,	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	.,		1
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	l _{OL1}	OL2	Іон	lin	l _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{ccl}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _{F1}	1	-	-2.1	-	-2.1	-	-2.1	mAdc	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	14	-	-	7*
	I _{F2}	1	-	-2.6	-	-2.6	-	-2.6	mAdc	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*
Leakage Current	IR	1	-	80	-	80	-	80	μ Adc	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 4, 5, 7 *
Breakdown Voltage	BVin	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7 *
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	T -	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	v _{OL1}	6	-	0.4	-	0.4	-	0.4	Vde	6	-	-	-	-	-	1	-	-	2, 4, 5	-	-	14	-	-	7*
	V _{OL 2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	6	-	-	-	-	1	-	-	2, 4, 5	-	-	-	14	-	7*
	v _{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	6	-	-	1	-	-	-	2, 4, 5	-	-	. 14	-	-	7
Short-Circuit Current	I _{SC}	6	-	-	-50	-125	-	-	m A	-	-	-	-	-	-	-	-	-	-	-	14	-	-		1,2,4,5,6,7*
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	16	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7 9, 10, 12, 13
Power Supply Drain	I _{PDH}	14	-	32	-	32	-	32	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7
	I _{PDL}	14	-	10	-	10	-	10	mAde	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7 9, 10, 12, 13
Switching Parameters										Pulse In	Pulse Out										14			2, 4, 5	7*
Turn-On Delay	t pd''0''	1,6	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	_	-	-	-	14	-	-	2,4,5	L
Turn-Off Delay	t pd''1''.	1,6	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*

^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

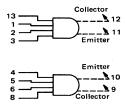
DUAL 4-INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL III MC3000 series

MC3030



This device consists of two independent 4-input AND gates. The outputs of each gate are available as ORing nodes. Using the MC3030 expander, with the MC3020 expandable gate, up to four AND gates can be ORed together.

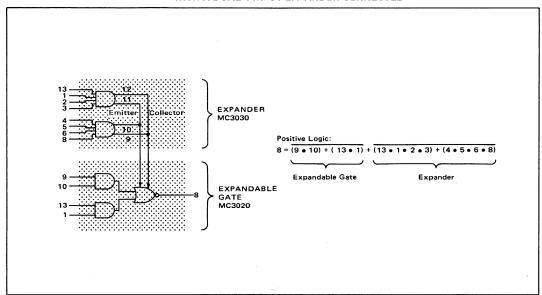


Input Loading Factor = 1

Full output loading factor of the expandable gate is maintained.

at expansion points.

APPLICATION: EXPANDABLE 2-WIDE 2-INPUT AND-OR-INVERT GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED



Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



						TEST	CURREN	IT/VO	LTAGE	VALUES	***************************************			
@Test		ı	nA											
Temperature	lc	l _{in}	l _D	V _R	V _{RH}	٧ _F	VEET	V _{EE2}	VIH	V _{IL}	V _{max}	V _{cc}	V _{ccl}	V _{CCH}
0°C	6.0	-	-	2.5	4.0	0.4	1.010	0.70	2.0	1.1	-	5. 0	4.5	5. 5
+25℃	6.0	1.0	-10	2.5	4.0	0.4	0.975	0.65	1.8	1. 1	7.0	5.0	4.5	5. 5
+75°C	6.0	-	-	2.5	4.0	0.4	0.935	0.55	1.8	0.9	-	5.0	4.5	5, 5

		Pin		MC	3030	Test Lim	its						TEST	CURE	RENT /	VOLTA	GE API	PI IFD T	O PINS	LISTED B	FIOW.			1
		Under	0	°C	+2	5°C	+7	5℃		<u> </u>	т —		T		1		1	1	0 11113		LLOW:			
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	١ _c	l _{in}	I _D	V _R	V _{RH}	V _F	VEET	V _{EE2}	V _{IH}	V _{IL}	V _{max}	Vcc	V _{ccι}	V _{CCH}	Gnd
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	2, 3,	1	-		-	-	-	-	14	-	7*
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	2, 3, 13	1	-	-	-	-	-	-	-	14	7*
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	2, 3, 7, 13*
Breakdown Voltage	BV _{in}	1	-	-	5.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-		-	-	14	2, 3, 7, 13*
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	7*
Output Output Voltage	V _{OL}	12	-	1.41	-	1.38	-	1.34	Vdc	12	-	-	-	-	-	11	-	1	-	-	-	14	-	7*
Emitter Current	I _{EO}	11	-	-300	-	-300	-	-300	μAdc	-	-	-	-	-	-	-	11	-	1		-	12, 14	-	7**
Collector Current	^I co	12	-	300	-	300	-	300	μAdc	-	-	-	-	-	-	-	11	1	-	-	-	12, 14	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	7, 0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,3,4,5, 6,7,8,13
Power Supply Drain * Ground inputs to ga	PDL	14	-	5.0	-	5. 0	-	5. 0	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-		1,2,3,4,5, 6,7,8,13

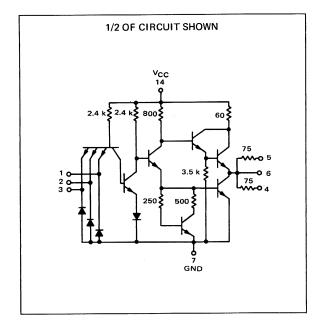
^{*} Ground inputs to gates not under test unless otherwise noted.

^{**} The inputs to both gates are ungrounded.

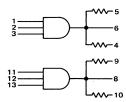
DUAL 3-INPUT 3-OUTPUT "AND" SERIES TERMINATED LINE DRIVER

MC3028

MTTL III MC3000 series



This device is a dual 3-input/3-output series-terminated AND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6, = $1 \cdot 2 \cdot 3$ Negative Logic: 4, 5, 6, = 1 + 2 + 3

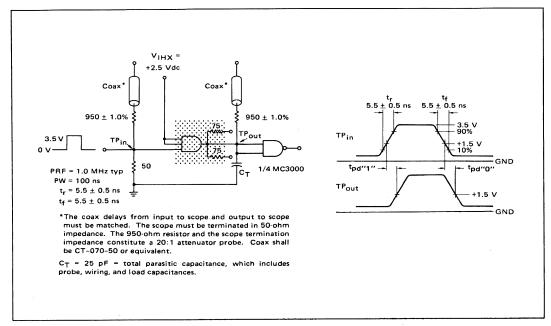
Input Loading Factor = 1

Output Loading Factor, Direct Output (Pins 6 & 8) = 10 minus the number of resistor-terminated outputs being used.

Output Loading Factor, Resistors (Pins 4, 5, 9, & 10) = 1

Total Power Dissipation = 56 mW typ/pkg Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one line driver. The other line driver is tested in the same manner. Further, test procedures are shown for only one input of the line driver being tested. To complete testing, sequence through remaining inputs.



									TEST	CURI	RENT/\	/OLTAC	E VAL	UES							
@Test					m	Α										Volts					
Temperature	I _{OL 1A}	I _{OL 1B}	l ^{OL 1C}	I _{OL 2A}	I _{OL 2B}	lol 2C	I _{OH A}	I _{OH B}	I _{OH C}	l _{in}	I _D	VIL	V _{IH}	V _F	V _R	V _{RH}	V _{max}	Vcc	V _{cc1}	V _{cch}	V _{IHX}
0°C	15.2	1.9	1.9	18, 4	2.3	2.3	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.5	4.0	-	5. 0	4.5	5. 5	-
+25°C	15.2	1.9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	15. 2	1.9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-

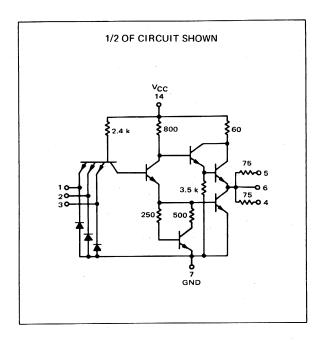
		Pin		M	C3028	Test Lir	nits		.,,,,			1		1 2.0	1 2.5		rest cui	DDENT /				TO DIA	•	ED BELOW	4.0		3.0	1 4.5	3.3	<u> </u>	1
		Under	0	°C	+2	5°C	+7	5°C		_		_					1231 (0)	MEITT /	1011	AUL AI	LILL	10 11	13 1.13	ED BELOW							_
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	I _{OL 1A}	I _{OL 1B}	lol 10	I _{OL 2A}	I _{OL 2B}	I _{OL 2C}	I _{OH A}	I _{OH B}	I _{OH C}	l _{in}	I _D	VIL	V _{IH}	V _F	V _R	V _{RH}	V _{mex}	Vcc	V _{ccl}	V _{CCH}	V _{IHX}	Gnd
input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	m Adc	-	-	-	-	-	-	-	-	-	-	T -	-	-	1	-	2,3*	-	-	14	-	-	7
	IF2	1	-	-2.3	-	-2.3	-	-2.3	mAde	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	2,3*	-	T -	-	14	-	7
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1		-	-		14	-	2, 3, 7
Breakdown Voltage	BVin	1	-	-	5.5	-	-	-	Vdc	-	-	-	-	-	1	-	-	-	1	-	-	-	-		•	†	-	-	14	-	2,3,7
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	•	-	-	14	-	-	7
Output Output Voltage	v _{OL1}	6	-	0.4	-	0.4	-	0.4	Vdc	6	5	4	-	-	-	-	-	-	-	-	1	-	-	-	2, 3*	-	-	14	-	-	7
	V _{OL2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	-	T -	6	5	4	-	-	-	-	-	1	-	-	-	2,3*	-	Ι-	-	14	-	7
	V _{OL 3}	5	-	0.5	-	0.5	-	0.5	Vdc	6	5	4	-	-	-	-	-	-	-	-	1	-	-	-	2, 3 *	-	-	14	-	-	7
	V _{OL 4}	5	-	0.5	-	0.5	-	0.5	Vdc	-	-	-	6	5	4	-	-	-	1-	-	1	-	-	-	2,3*	-	-	-	14	-	7
	v _{он}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	-	-	-	-	6	5	4	-	-	-	1	-	-	2,3*		-	14	-	-	7
Short-Circuit Current	I _{SC}	6	-	-	-30	-100	-	-	mAde	-	-	-	-	-	-	-	-		-	-	-	-	-	-	1, 2, 3*	-	14	-	-	-	6,7
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	18	-	-	mAde	-	-	-	-	-	-	-	-	-	-	-	-		-	-	1, 2, 3, 11, 12, 13	14	-	-	-	-	7
Power Supply Drain	I _{PDH}	14	-	12	-	12	-	12	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	-	14	-	-	-	7
	I _{PDL}	14	-	24	-	24	-	24	mAde	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 7 11, 12, 13
Switching Parameters										Pulse In	Pulse Out																				
Turn-On Delay	tpd"0"	1, 6	ļ.		-	12	-	L-	ns	1			ļ	<u> </u>	-	<u> </u>	-	-	-	_	<u> </u>	_	_	-	•		14	-	-	2, 3	7
Turn-Off Delay	t _{pd"1"}	1,6	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	-	-	-	•	-	14	-	-	2,3	7

^{*}Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to ${\rm V}_{\rm RH}$.

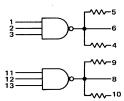
DUAL 3-INPUT 3-OUTPUT "NAND" SERIES TERMINATED LINE DRIVER

MTTL III MC3000 series

MC3029



This device is a dual 3-input/3-output series-terminated NAND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6 = $1 \cdot 2 \cdot 3$ Negative Logic: 4, 5, 6 = 1 + 2 + 3

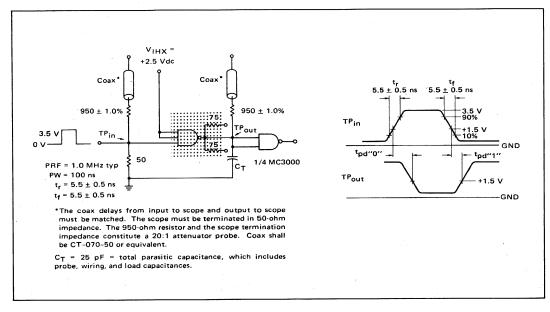
Input Loading Factor = 1

Output Loading Factor, Direct Output (Pins 6 and 8) = 10 Minus The Number of Resistor-Terminated Outputs Being Used.

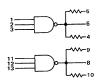
Output Loading Factor, Resistors (Pins 4, 5, 9 and 10) = 1

Total Power Dissipation = 44 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one line driver. The other line driver is tested in the same manner. Further, test procecures are shown for only one input of the line driver under test. To complete testing sequence through remaining inputs.



									TEST	CURR	ENT/V	OLTAG	E VAL	UES							
@Test					m	A										Volt	s				
Temperature	l _{OL 1A}	I _{OL 18}	l _{OL 1C}	I _{OL 2A}	I _{OL 28}	I _{OL 2C}	I _{OH A}	I _{OHB}	I _{OH C}	l _{in}	ID	٧ _{IL}	V _{IH}	٧,	V _R	V _{RH}	V _{max}	V _{cc}	V _{ccl}	V _{cch}	V _{IHX}
0°C	15.2	1.9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.5	4.0	-	5. 0	4.5	5. 5	-
+25℃	15.2	1.9	1.9	18.4	2.3	2.3	-1.8	-0, 1	-0.1	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75℃	15. 2	1, 9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5. 5	-

					MC3	029 Tes	t limits		,,,,			1	1 10.1	1	1 0.0		TECT CUI	DENT (VOLTA	Cr 40		TO 011			1 4.0		5.0	4.5	3.5	<u> </u>	1
		Pin Under	0	°C		5°C	+7		Γ	L			,				EST CUI	KKENI /	VOLIA	IGE AP	PLIED	IU PIN	12 FI21	ED BELOW	:						_
Characteristic	Symbol	Test			Min	Max	Min	Max	Unit	I _{OL 1A}	I _{OL 18}	I _{OL 1C}	I _{OL 2A}	I _{OL 28}	l _{OL 2C}	I _{OH A}	I _{OH B}	I _{OH C}	l _{in}	I _D	٧ _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	Vcc	V _{ccı}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	T -	-	-	-	-	-	-	-	-	-	-	1	-	2, 3	-	-	14	-	-	7*
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	2,3	-	-	-	14	-	7*
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1		-	-	-	14	-	2, 3, 7*
Breakdown Voltage	BVin	1	-	-	5.5	-	Ŧ	-	Vdc	-	-	-	-	T -	-	-	-	-	1	-	-	-	-	-	-	-	-	-	14		2, 3, 7*
Clamp Voltage	v _D	1	-	-	-	-1.5	, -	-	Vdc	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	- ;	-	-	14	-	· ·	7*
Output Output Voltage	V _{OL 1}	6	-	0.4	-	0.4	-	0.4	Vdc	6	5	4	-	-	-	-	-	-	-	-	-	1	-	-	2,3	-	-	14	-	-	7*
	V _{OL2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	-	-	6	4	5	-	-	-	-	-	-	1	-	-	2, 3	-	-	-	14	-	7*
	V _{OL 3}	5	-	0.5	-	0.5	-	0, 5	Vdc	6	5	4	-	-	-	-	-	-	-	-	-	1	-		2,3	-	-	14	-	-	7*
	V _{OL 4}	5	-	0, 5	-	0.5	-	0.5	Vdc	-	-	-	6	4	5	-	-	-	-	-	-	1	-		2, 3	-	-	-	14	-	7*
	V _{ОН}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	-	-	-	-	6	4	5	-	-	1	-	-	-	2, 3	-	-	14	-	-	7*
Short-Circuit Current	I _{SC}	6	-	-	-30	-100	-	•	mAdc.	-	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	14	-	-		1, 2, 3, 6, 7 *
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	12	-	-	mAdc		-	-	-	-	-	-	-	-	-	-	-				-	14	-	-	-		1, 2, 3, 7, 11, 12, 13
Power Supply Drain	I _{PDH}	14	-	18	-	18	-	18	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	-	14	-	-	-	7
	I _{PDL}	14	-	9	-	9	-	9	mAde	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 7, 11, 12, 13
Switching Parameters Turn-On Delay	t _{pd"0"}	1,6	_	_		10		_	ns	Pulse In	Pulse Out				_	_	_				_	_	_	-		_	14		_	2, 3	7*
Turn-Off Delay		1,6	+	 -	-	10	<u> </u>	-	ns	1	6	-	H-	<u> </u>	<u> </u>	<u> </u>	-	-	-		_	_					14			2,3	7*
	pd"1"	1,0	L			10	<u> </u>	Ĺ	5	L ^	L	l	_			-	_	-			1	_									

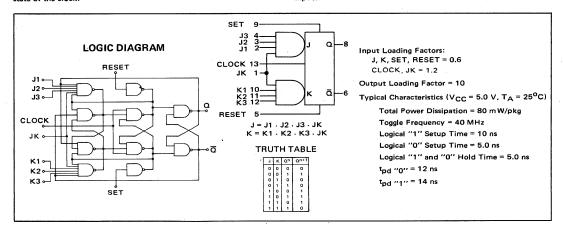
^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

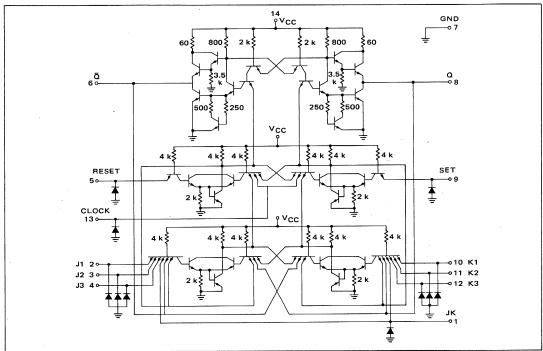
"AND" J-K FLIP-FLOP

MC3050

This J-K flip-flop triggers on the positive edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and a K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct SET and RESET are provided to permit presetting data, such as initial conditions into the flip-flop. The direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at the J and K inputs any time in a clock cycle, except during the interval of time between the Set-up and Hold times. The inputs are inhibited when the clock is high; data is entered into the input steering section of the flip-flop when the clock goes low. The input steering section of the flip-flop continually reflects the input state when the clock is low. Data present during the time interval between the Set-up and Hold times is transferred to the bistable section on the positive edge of the clock and the outputs Ω and $\bar{\Omega}$ respond accordingly. The flip-flop can be set or reset directly by applying the high state to the SET or RESET inputs.





OPERATING CHARACTERISTICS

High state data must be present 17 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

Positive edge triggering: When the clock goes from the low state to the high state, the information in the input steering section is transferred to the bistable section.

The direct SET and RESET inputs may be used any time, regardless of the state of the clock. If these inputs are not used THEY MUST BE TIED TO GROUND.

Unused Inputs:

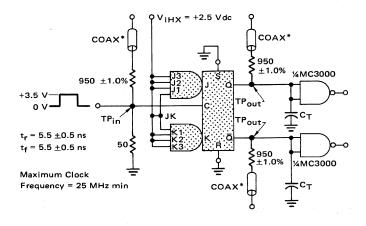
JK input MUST be in the high state to enable the clocked inputs. When the JK input is not used, it should be tied to a voltage between 2.0 and 5.5 Vdc.

Unused J inputs should be tied to used J inputs, the used JK input, $\overline{\Omega}$, or a voltage between 2.0 and 5.5 Vdc

Unused K inputs should be tied to used K inputs, the used JK input, Ω , or a voltage between 2.0 and 5.5 Vdc.

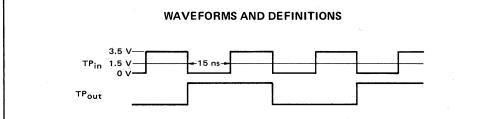
Unused SET and RESET inputs MUST be tied to ground.

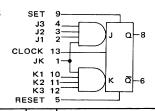
FIGURE 1 - MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.





						TEST C	URREN	T/V0	LTAG	E VALUES				
@ Test		n	1A							Volts				
Temperature	l _{OL}	Гон	l _{in}	2I _{in}	I _D	VIL	V _{IH}	V _F	\forall_{R}	V _{RH}	V _{max}	V_{CC}	V _{CCL}	V _{CCH}
0°C	23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5,5
+25°C	23	-2.0	1.0	2.0	10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
+75°C	23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5

		Pin		MC		Test L	imits						TEST	CUR	RENT/\	/OLTA	GE AP	PLIED	TO PINS LISTED B	ELOW:				
	1	Under	0	°C	+2	5°C	+7	75°C		├.	Γ.	г. –	T	Γ.	T.,	1	I	T 1			T.,	T.,	<u></u>	
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	OL	l _{ОН}	lin	21 _{in}	l _D	V _{IL}	VIH	V _F	V _R	V _{RH}	V _{max}	Vcc	V _{CCL}	V _{CCH}	Gnd
Input Forward Current	I _{FJ}	2 3	-	-1.5	-	-1.5 	-	-1.5	mAdc	-	- -		-	- -	-		2 3	-	1,3,4,5 1,2,4,5	-	- ,	-	14	7,9,13
	FK	10 11 12	-	-1.5	-	-1.5	- - -	-1.5	mAdc	-			-	- - - -	-	-	10 11 12	-	1,2,3,5 1,9,11,12 1,9,10,12 1,9,10,11	-	- " - "	, = , := , := , :=	14	5,7,13
	IFC	13	-	-3.0	-	-3.0	-	-3.0	m Adc	-	-	-	-		-	-	13	-	-	-	-	-	14	1,5,7,9
	I _{FJK}	1	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	1	-	2,3,4,10,11,12	-		-	14	5,7,9,13
:	IFS	9	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-		1	9	-	5	-	-		14	7
	I_{FR}	5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-		5	-	9	-	-,	- 1	14	7
Leakage Current	I _{RJ}	2 3 4		80		80	-	80	μAdc ↓	- -	-		- 1	-	-	-	-	2 3 4	9	- , - ,	-	-	14	1,3,4,5,7 1,2,4,5,7 1,2,3,5,7
	IRK	10 11 12	-	80	-	80	-	80	μAdc	- - -	- - -	-	- - -	- -		-	-	10 11 12	5 	- - -	-	-	14	1,7,9,11,12 1,7,9,10,12 1,7,9,10,11
	IRC	13	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	-	13	1,2,3,4,5,10,11,12	-	-	-	14	7,9
	I _{RJK}	1	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	-	1	9	-		-	14	2,3,4,5,7,10,11,12
	IRS	9	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	9	.			-	14	7
	I_{RR}	5	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	5	-	-	-	-	14	7

ELECTRICAL CHARACTERISTICS (continued)

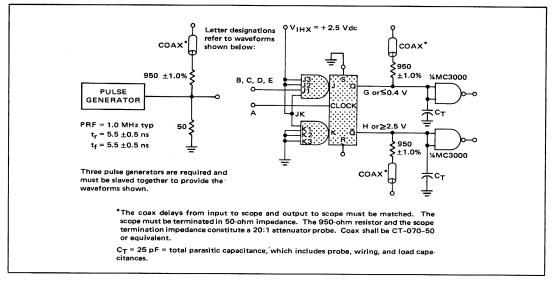
						TEST C	URREN	T/V0	LTAG	E VALUES				
@ Test		n	Α							Volts				
Temperature	lor	Іон	l _{in}	21 _{in}	I _D	V _{IL}	V _{IH}	٧ _F	V _R	V _{RH}	V _{max}	٧ _{cc}	V _{CCL}	V _{CCH}
0°C	23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4. 0	-	5.0	4.5	5.5
+25°C	23	-2.0	1.0	2.0	10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
+75°C	23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4. 0	-	5.0	4.5	5.5

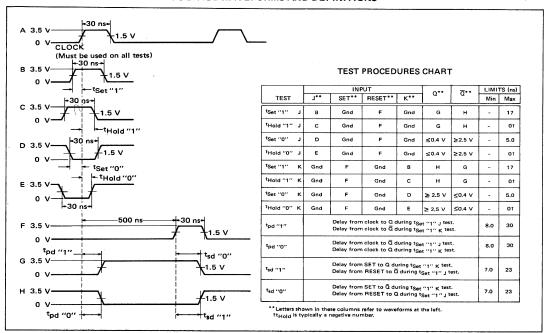
		Pin		MC	3050	Test L	imits		.,,, с		l		TEST	CUR	RENT/\	/OLTA	GE AP	PLIED	TO PINS LISTED BI	ELOW:				
		Under	0	°C	+2	25°C	+7	75°C			r	Γ.										т		0.1
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	loL	l _{ОН}	l _{in}	21 _{in}	l _D	VIL	VIH	V _F	V _R	V _{RH}	V _{max}	Vcc	VCCL	V_{CCH}	Gnd .
Breakdown Voltage	BVin	2 3	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	-	9	-	-	-	14	1,3,4,5,7 1,2,4,5,7
		4	-	-		-	-	-		-	_	4	-	-	-	-	-	-	 	-	-	-		1,2,3,5,7
		10	-	-	ŀ	-	-	-		-	-	10	-	-	-	-	-	-	5	-	-			1,7,9,11,12
		11	-	-		-	-	-		-	-	11	-	-	-	-	-	-	. ↓	-	-	-		1,7,9,10,12
		12 13	-			-	-	-		-	-	12	13	-	-	-	-	-	1,2,3,4,5,10,11,12	-	-	-		1,7,9,10,11 7,9
		13	_	-		_	_] -		_	-	-	1	-	-	-	-	-	9	-	-	-		2,3,4,5,7,10,11,12
		9	-	-	Ш	-	-	-	1 1	-	-	9	-	-	-	-	-	-	-	-	-	-		7
		5	-	-	1	-	-		7		-	5	- '	ļ	-	-	-		-	-	-	<u> </u>	7	7
Clamp Voltage	v _D	2		-	-	-1.5	-	-	Vdc	-	-	-	-	2	-	-	-			-	-	14	-	7
		3	-	-	-		-	-		-	-	-	-	3 4	-		<u>-</u>	-	-	-	-	1 1	-	
		10	_	-	-		-	1 -		_	_	_	_	10	-	-	-	-	_	[-		_	
		11	-	-	-		-	-		-	-	-	-	11	-	-	-	-	-	-	-		-	
		12	-	-	-		-	- '		-	-	-	-	12	-	-	-	-	-	-	-		-	
		13	-	-	-		-	-		-	-	-	-	13	-	-	-	-	-	-	-		_	
·		9	_	-	-		-	1 -		[_	_	_	9	[-	-	-	_	-	_		_	
		5	_	-	_	🛊	-	- "	🕴	-	-	-	-	5	-	-	-	-	-	-	-	*	-	*
Output	V _{OL}	6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	5	9	-	T -	-	-	-	-	14	7,13
Output Voltage		8	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	9	5	-	-	-	-	-	1	14	7,13
	v _{oh}	6 8	2.5	-	2.5	-	2.5	-	Vdc Vdc	-	6 8	-	-	1 -	9	5 9	-	-	- \	-	-	14	_	7,13 7,13
a a			 	<u> </u>	-30	-100		<u> </u>	mAdc	<u> </u>	0	- -	 -	+-	J	-	-	├	5	- -	14	+	-	
Short-Circuit Current	sc	6 8	-	-	-30	-100	-	-	mAdc mAdc	-	-	-	=	=		-	-	-	9	-	14	-	-	6,7,9 5,7,8
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	_	-	-	35	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,5,7,13
Power Supply Drain	I _{PD}	14	-	26	Ξ	26	<u> </u>	26	mAdc	-	-	-	-	<u> </u>	<u> </u>	Ŀ	-	-	-		14		-	1,5,7,13

OPERATING CHARACTERISTICS (continued)

FIGURE 2 - SWITCHING TIME TEST CIRCUIT

(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)





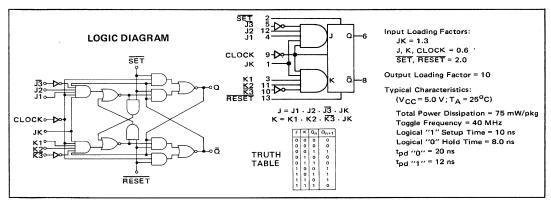
MTTL III MC3000 series

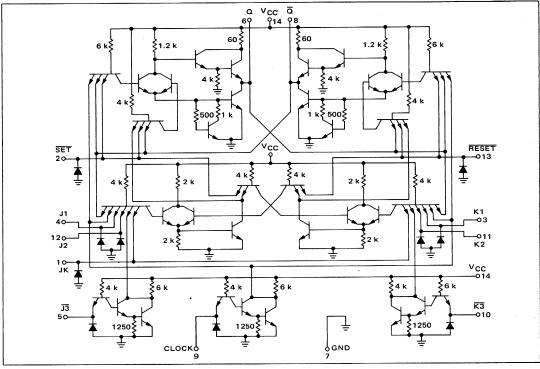
"AND" INPUT JĪ-KR Flip-Flop

MC3052

The MC3052 is a master-slave J-K flip-flop that triggers on the positive edge of the clock. The flip-flop has an AND input configuration consisting of two J-inputs and a J-input ANDed together and two K-inputs and a K-input ANDed together. An enable input (JK) is also provided consisting of an additional J and K input internally connected together. This input provides gating in addition to the clock for the clocked inputs (J, J, K and K) or an additional logic input (JK) for use in counters or certain other applications. A direct SET and RESET are provided to enable presetting data into the flip-flop such as initial conditions. The direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information is normally applied to, or changed at, the clocked inputs while the clock is in the high state, since the inputs are inhibited under this condition. Information may be stored in the master flip-flop section when the clock goes low. Once input data has been stored in the master flip-flop section it cannot be removed (or changed) by means of the clocked inputs. The direct \overline{SET} or \overline{RESET} provide the only means of removing previously stored information. The state of the master flip-flop is transferred to the slave flip-flop section on the positive transition of the clock and the outputs respond accordingly. The flip-flop can be set or reset directly by applying the low state to the direct \overline{SET} or \overline{RESET} inputs.





ELECTRICAL	SE				\supset	٦.																			
CHARACTERISTI	ics 3	3 ,5 Do).		o—6			_					T	EST C	URRE	IT/V	OLTAG	E VALUES						
	CLOC	к 9		\preceq				(i	@ est		m	ıA							Volts					-	
		к 1—	•L						rature	lor	loh	l _{in} .	21 _{in}	I _D	VIL	V _{IH}	٧ _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}		
	Ķ	1 3 2 11 3 10 Do),	<	ā s			0°C	23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5		
	RESE			_/	\Box	_			+25°C	23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5		
									+75℃	23	-2.0				0,9	1.8	0.4	2, 5	4.0	-	5.0	4.5	5.5	1	
		Pin	<u> </u>	O°C		Test L		′5°C				TES	T CURI	RENT/	VOLT	AGE A	PPLIE	D TO I	PINS LISTED BEL	0W:					
Characteristic	Symbol	Under Test		Max		Max		Max	Unit	l _{OL}	Гон	lin	2I _{in}	ID	V _{IL}	VIH	٧ _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}	P,*	Gnd
Input Forward Current	1.																			-					
Forward Current	I _F J	4 12	-	-1.5 -1.5	-	-1.5 -1.5	-		mAdc mAdc	-		-	-	-	-	-	4 12	-	1,12 1,4		-		14 14	-	5,7,9,13 5,7,9,13
	I _{FK}	3 11	-	-1.5 -1.5	-	-1.5 -1.5	-		mAdc mAdc	-	-	-	-	- 1	-	-	3 11		1,11 1,3	-	-	-	14 14	-	2,7,9,10 2,7,9,10
	$I_{F\overline{J}}$	5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	5	-	- :	-	-	-	14	-	7
	$I_{\overline{FK}}$	10	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	10	-	-	-	-	-	14	1-1	7
	I _{FC}	9	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	9	-	-	-	-	-	14	-	7
	I_{FJK}	1	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	1	-	3,4,11,12	-	-	-	14	- 1	2,5,7,9,10,13
	I _{FS}	2	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-		2	-	-	-	-	-	14	-	7,9,13
	$I_{F\overline{R}}$	13	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-	-	13	-		-	-	-	14	-	2,7,9
Leakage Current	I_{RJ}	4 12	-	80 80	-	80 80	-	80 80	μAdc μAdc	-	-	-	-	-		-	-	4 12	5,9 5,9	-	-	-	14 14	-	1,2,7,12 1,2,4,7
	IRK	3 11	-	80 80	-	80 80	-	80 80	μAdc μAdc	-	-	-	-	-	-	-	-	3 11	9,10 9,10	-	-	-	14 14	-	1,7,11,13 1,3,7,13
	$I_{R\overline{J}}$	5	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	5	-	-	-	-	14	-	7
	I _{RK}	10	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	- 1 - 1 - 1	10	-	-	-	-	14	-	7
	IRC	9		80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	9	-	-	-	- 1	14	-	7
	I _{RJK}	1	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	-	1	5,9,10	-	-	-	14	- 1	3,4,6,7,8,11,12

1,4,10,12,13

1,2,3,5,11

13

14 9

14

3,5,7,11

4,7,10,12

13 4.0 V (V_{RH}) *Pulse is used to set flip-flop in desired state. $P_1 = -$

2

 $I_{R\overline{R}}$

140

140

140

140

140 μAdc

140 μAdc

ELECTRICAL CHARACTERISTICS (continued)

[T	EST C	URREN	IT/V	OLTAGE	VALUES				
@ Test		n	nΑ							Volts				
Temperature	lor	Гон	lin	2I _{in}	I _D	VIL	V _{IH}	V _F	V _R	V _{RH}	V _{max}	٧ _{cc}	V _{CCL}	V _{CCH}
o°c	23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5
+25°C	23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
+75°C	23	-2.0	T-	-	-	0, 9	1.8	0.4	2.5	4.0	T -	5.0	4.5	5.5

		Pin				Test L						TES	T CUR	RENT	VOLT	AGE A	PPLIE	D TO I	PINS LISTED BEL	OW:					
		Under)°C	+2	5°C	+7	5°C			· ·		-						T 1/	I.,	I.,				Gnd
	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	lor	I _{ОН}	lin	$2l_{in}$	l _D	٧ _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	Vcc	VCCL	V _{CCH}	P ₁ *	Gna
Breakdown Voltage	BV _{in}	4	-	-	5.5	-	-	-	Vdc	-	-	4	-	-	-	-	-	-	5,9	-	-	-	14	-	1,2,7,12
		12 3	-	-		-	-	-		-	-	12 3	-	-	-	-	-	-	5,9	-	-	-		-	1,2,4,7 1,7,11,13
		3 11	-	-		-	-	-		-	_	11	-	-	-	-	-	_	9,10 9,10	-	_			- 1	1,3,7,13
		1	-	-		-	-	-		-	-	-	1	-	-	-	-	-	2,5,9,10,13	-		-		-	3,4,6,7,8,11,12
		2	-	-		-	- 1	-		-	-	-	2	-	-	-	-	-	1,4,10,12,13	-	-	-		9	3,5,7,11
		13	-	-	.	-	-	-		-	-	-	13	-	-	-	-	-	1,2,3,5,11	-	-			9	4,7,10,12
		5 9	-	-		-	-	-		-		5 9	-		-	-	-	-	1	-	1 -	-		-	7
		10	-	-	, 🔻	-	-	-	+	_	-	10	-	-		-	-	-	-	-	-	-	+	-	7
Clamp Voltage	v _D	4	-	-	-	-1.5	-	-	Vdc	-	-	-	-	4	-	-	-	-	-	-	-	14	-	-	7
	ъ	12	-		-		-	-		-	-	-	-	12	-	-	-	-	-	-	-	1	-	-	
		3 11	-	-	-			-		-	-	-	-	3 11	-	-	-	-	1 1	1 :	-		_	1	
		5	-		_			_		_	_	-	_	5	_	-	_	_]]	_	-		-	-	
		10	-	-	-		-	-		-	-	-	-	10	-	-	-	-	<u> </u>	-			-	-	
·		9	-	- ,	-		-	-		-	-	-	1.5	9	_	- 1	-	-	<u> </u>	-			1 :	-	
		2	-	-	_			-		-	-	-	-	2	-	-	-	-	-	-	-			-	
		13	-	-		7	-	-	7	-	-	-	-	13			-	-	-		-	<u>'</u>	-	-	
Output										,					10			_		· _	_	_	14		7.0
Output Voltage	VOL	6 8	- 1	0. 4 0. 4	-	0.4	-	0. 4 0. 4	Vdc Vdc	6 8	-		-	-	13 2	2 13	-	-	-	-	_	_	14	-	7,9 7,9
	v _{OH}	6 8	2. 5 2. 5	-	2.5 2.5	-	2.5 2.5	-	Vdc Vdc	-	6 8	-	- 1	-	2 13	13 2	-	-	-	-	-	14 14	-	-	7,9 7,9
Short-Circuit Current	I _{SC}	6	-	-	-30 -30	-100 -100	-	-	mAde mAde	- 1	-	-	-	-	-	-	-	-	-	-	14 14	-	-	-	2,6,7 7,8,13
Power Requirements						1					-		<u> </u>	 							T			T	
(Total Device)												l													
Maximum Power Current	I _{max}	14	-	-	-	42	-	-	mAdc	-	-	-	-"	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7,9,10,11,12,13
Power Supply Drain	I_{PD}	14	-	30	1	30	-	- (V	mAdc	-	-	-	-	-	-	-	-	-	-	-	14		-	-	1,2,5,7,9,10

Pulse is used to set flip-flop in desired state. $P_1 = 4.0 \text{ V}$ (V_{RE}

OPERATING CHARACTERISTICS

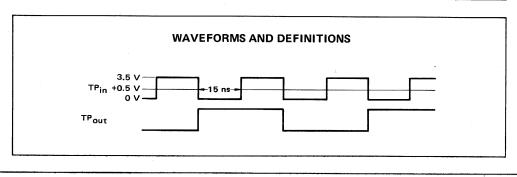
Data should be present prior to the negative clock transition. If data is changed from a "1" to a "0" while the clock is in the low state, the flip-flop will not recognize this new data state.

The application of a low level to the SET input sets Q high and low level on the RESET input resets Q low. These functions may be performed at any time without regard to the clock area.

Positive edge triggering — When the clock goes from the low to the high state, the information stored in the master flip-flop section is transferred to the slave flip-flop section thus appearing at the outputs. When the clock is in the high state, the inputs are inhibited.

Unused J, K, and JK inputs should be tied together with used inputs, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc. The unused \overline{J} and \overline{K} inputs must be tied to ground. The unused \overline{SET} and \overline{RESET} inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

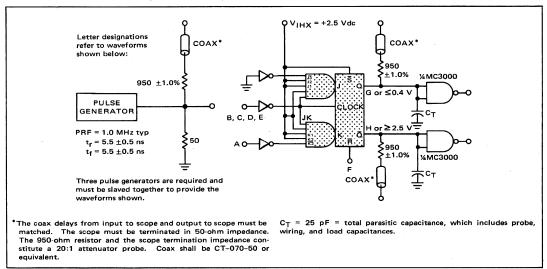
FIGURE 1 - MAXIMUM CLOCK FREQUENCY TEST CIRCUIT V_{IHX} = +2.5 Vdc COAX* **∮**950 ±1.0% 14MC3000 950 ±1.0% +3.5 V $\mathcal{L}_{\mathsf{TP}_{\mathsf{out}}}$ TPin-0 V TPout 50 t_r = 5.5 ±0.5 ns \$950 t_f = 5.5 ±0.5 ns ±1.0% 14MC3000 Maximum Clock Frequency = 25 MHz *The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent. C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

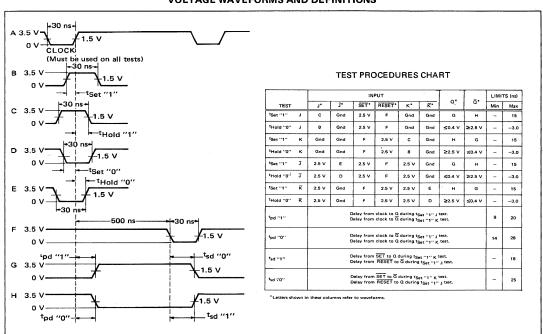


OPERATING CHARACTERISTICS (continued)

FIGURE 2 - SWITCHING TIME TEST CIRCUIT

(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)

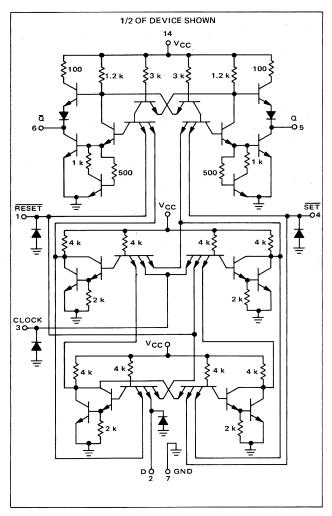




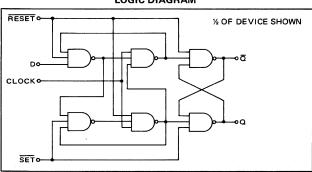
MTTL III MC3000 series

DUAL TYPE D FLIP-FLOP

MC3060



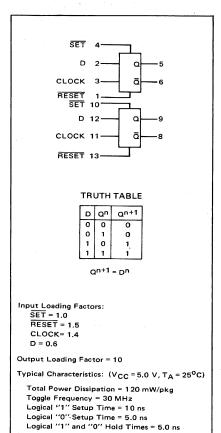
LOGIC DIAGRAM



The MC3060 dual flip-flop triggers on the positive edge of the clock and performs the Type D flip-flop logic function. This device consists of two completely independent Type D flip-flops, both having direct SET and RESET inputs for asynchronous operations such as parallel data entry in shift register applications.

Information may be applied to, or changed at, the D inputs any time during the clock cycle except during the time interval between the Set-up and Hold times. The clocked inputs are inhibited when the clock is high and data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the Set-up and Hold times is transferred to the bistable section on the positive edge of the clock, and the outputs Q and $\overline{\rm Q}$ respond accordingly.

The flip-flop can also be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct $\overline{\text{SET}}$ or $\overline{\text{RESET}}$ inputs.



t_{pd} "0" = 17 ns t_{pd} "1" = 15 ns

SET **ELECTRICAL CHARACTERISTICS** Test procedures are shown for only one flip-flop. The other flip-flop is tested in CLOCK TEST CURRENT/VOLTAGE VALUES the same manner. RESET mΑ Volts Test SET VCCL ٧_{cc} VCCH VIH VRH l_D OL ОН Temperature 0°C 23 2.0 0.4 2.5 5.0 4.5 -2.0 1.1 4.0 5.5 ₫-8 CLOCK 11-+25°C 23 -2.0 1.0 2.0 -10 1.1 1.8 0.4 2.5 4.0 7.0 5.0 4.5 5.5 +75°C 23 0.9 RESET 13--2.0 1.8 0.4 2.5 4.0 5.0 4.5 5.5 MC3060 Test Limits TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: 0°C +25°C Under +75°C V_{CCH} V_{IH} VRH V_{max} V_{cc} VCCL P Gnd Characteristic Symbol Test Min Max Min Max Min Max Unit lor OH Input Forward Current -3.0-3.0 -3.0 mAdc 3 1 14 I_{FC} 2,4,7,11 2 -1.5 -1.5 FD -1.5 mAdc 2 1,4 14 3,7,11 4 -2.3 -2.3 -2.3 mAdc 4 1 14 I_{FS} 2,3,7,11 1 -3.4 -3.4 -3.4 I_{FR} mAdc 1 2,4 14 3,7,11 Leakage Current I_{RC} 3 110 110 110 μAdc 3 4 14 1,2,7,11 2 80 80 80 μAdc I_{RD} 2 3,4 14 1,7,11 I_{RS} 4 110 110 110 μAdc 4 1,2 14 3 7.11 1 140 140 140 I_{RR} μAdc 4 14 3 2,7,11 BV_{in} Breakdown Voltage 5.5 Vdc 3 3 14 1,2,7,11 2 2 3,4 1,7,11 4 4 1,2 3 7,11 3 2,7,11 4 Clamp Voltage -1.5 Vdc 3 14 7,11 2 4 1 1 Output Output Voltage 0.4 0.4 Vdc v_{ol} 0.4 . 4 1 2,3,7,11 0.4 0.4 0.4 Vdc 5 1 4 14 2,3,7,11 2.5 2.5 v_{OH} 2.5 Vdc 1 4 14 2,3,7,11 5 2.5 2.5 2.5 Vdc 4 5 14 2,3,7,11 Short-Circuit Current -20 I_{SC} -60 mAde 4 1 14 6,7,11 -20 -60 5 mAdc 4 14 5,7,11 Power Requirements (Total Device) Maximum Power 14 42 Imax mAdc 1.13 14 3,4,7,10,11 Supply Current Power Supply Drain 14 29 29 mAdc 4,10 14 1,3,7,11,13

^{*} Pulse is used to set flip-flop in desired state. $P_1 = \frac{4.0 \text{ V (VRH)}}{0 \text{ V}}$. If pin is also in another column, the pin must be returned to that voltage or current for measurement.

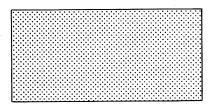
OPERATING CHARACTERISTICS

Data must be present 15 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

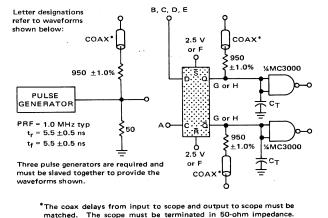
The direct SET and RESET inputs may be used at any time as they completely override the clock.

Positive edge triggering: When the clock goes from the low to the high state, the information in the input steering section is transferred to the bistable section.

Unused inputs should be tied to a voltage between 2.0 and 5.5 Vdc.



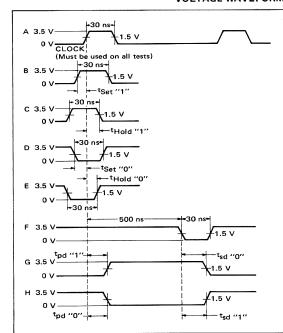
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

 $\mbox{C}_{\mbox{\scriptsize T}}$ = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

			INPL	JT			LIMI	TS (ns)
TEST		D*	SET*	RESET*	a*	₫*	Min	Max
^t Set "1"	D	В	2.5 V	F	G	н	-	15
tHold "1"	D	С	2.5 V	F	G	Ι	-	5.0
^t Set "0"	D	D	F	2.5 V	н	G	-	15
^t Hold "0"	D	E	F	2.5 V	н	G	-	5.0
^t pd "1"		1	Set "1"	n clock to (_	10	25
^t pd "0"		1	Set "0"	n clock to (10	25
^t sd "1"			Set ''0''	n RESET to			5.0	20
^t sd ''0''		1	Set "0"	n RESET to			5.0	20

^{*}Letters shown in these columns refer to waveforms at left.

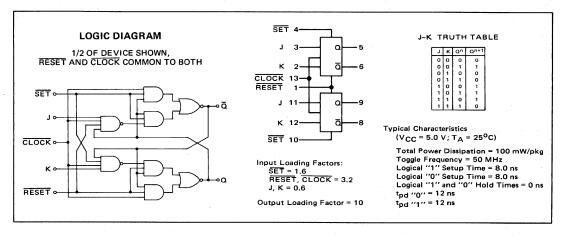
MTTL III MC3000 series

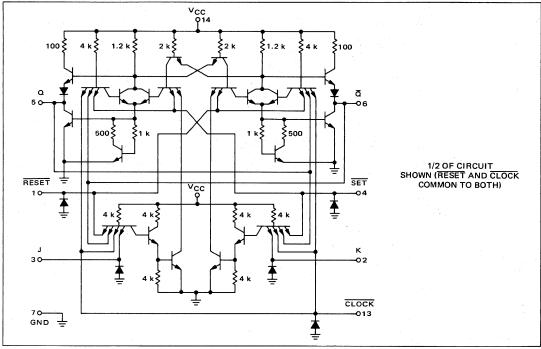
DUAL J-K FLIP-FLOP

MC3061

The MC3061 dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct SET input in addition to the common direct RESET input. These direct inputs provide a means of resetting a group of flip-flops such as a register which may be followed by the presetting of a data pattern. The clock input for this device is common for both flip-flops, making it particularly useful in registers or other common clock applications.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between the Setup and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between the Setup and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the $\overline{\text{SET}}$ input. In addition, both flip-flops may be reset simultaneously by using the common $\overline{\text{RESET}}$ in a similar manner.





Test procedures are shown for only one flip-flop plus the inputs common to both flip-flops. To complete testing, sequence through the remaining inputs in the same manner.



					TES	ST CUF	RENT	VOLT	AGE V	ALUES									
@ Test		m	A			Volts													
Temperature	loL	l _{он}	l _{in}	21 _{in}	l _D	V _{IL}	VIH	V _F	V _R	V _{RH}	V _{max}	V_{cc}	VCCL	V_{CCH}					
0°C	23	-2.0	-	- '	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5					
+25°C	23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5					
+75°C	23	-2.0	-	-		0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5					

		Pin		MC3061 Test Limits						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:															
		Under	0			5°C		′5°C		<u> </u>										v		lv.	14	D *	Gnd
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	lor	l _{ОН}	lin	2l _{in}	l _D	V _{IL}	V _{IH}	٧ _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}	P ₁ *	Gna
Input Forward Current	I_{FJ}	3	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	3	-	1,4,13		-	- 1	14	1	2,7,10
	I _{FK}	2	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	2	-	1,4,13	-	-	-	14	4	3,7,10
	I _{FR}	1	-	-3.5	-	-3.5	-	-3.5	mAdc	-	-	-	-	-	-	-	1	-	3,4,13	-	-	-	14	-	2,7,10
	I _{FS}	4	-	-1.8	-	-1.8	-	-1.8	mAdc	-	-	-	-	-	-	-	4		1,2,13	-	-	-	14	-	3,7,10
	I _F C	13	-	-5.7	-	-5.7	-	-5.7	mAdc	-	-	-	-	-		-	13	-	1,2,3,11,12	-	-	-	14	4,10	7
Leakage Current	I _{RJ}	3	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	1-	3	2,4	-	-		14	-	1,7,10,13
	I _{RK}	2	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	2	1,3	-	-	-	14	-	4,7,10,13
	I _{RR}	1	-	230	-	230	-	230	μAdc	-	-	-	-	-	-	-	-	1	2	-	-	-	14	1	3,4,7,11,13
	I _{RS}	4	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	-	4	. 3	-	-	-	14	4	1,2,7,10,13
	I _{RC}	13	-	290	-	290	-	290	μAde	-	-	-	-	-	-	-	-	13	-	-	- 1	-	14	-	1,2,3,4,7,10,11,12
Breakdown Voltage	BV _{in}	3 2 1 4 13	- - - -	- - - -	5.5	-	-		Vdc	- - - -	- - - -	3 2	- 1 4 13		-	-		-	2,4 1,3 2 3		-		14	- 1 4	1,7,10,13 4,7,10,13 3,4,7,11,13 1,2,7,10,13 1,2,3,4,7,10,11,11
Clamp Voltage	v _D	3 2 1 4 13		- - - -	-	-1.5	-		Vdc	-	-	-		3 2 1 4 13	-		- - -	-	- - - -	-		14			7,10
Output Output Voltage	v _{OL}	5	-	0.4 0.4	-	0.4 0.4	-	0.4 0.4	Vdc Vdc	5 6		-	7 <u>-</u>	• •	1 4	4	-	-		- -	- 1 -	-	14 14	1 4	7,10 7,10
	v _{он}	5 6	2.5 2.5	-	2.5 2.5	-	2.5 2.5	=	Vdc Vdc	-	5 6	-	-	1 1	4	1 4	-	-	-	-	-	14 14	-	4	7,10 7,10
Short-Circuit Current	I _{SC}	5 6	-	-	-20 -20	-60 -60	-	-	mAdc mAdc	-	-	-	-	1.1	-	-	-	-	-	-	14 14		-	-	4,5,7,10 1,6,7,10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	42		-	mAde	-	-	-	-		-	- 1	-	- -	- '	14	-	-	-	-	4,7,10
Power Supply Drain	I _{PD}	14	-	30		30	-	30	mAdc	-	-	-	-	-	-	-	-	-		-	14	-	-	-	1,7

^{*}Momentarily ground pin prior to taking measurement. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

OPERATING CHARACTERISTICS

High state data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

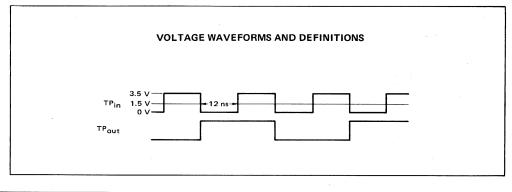
The direct \overline{SET} (individual) inputs and \overline{RESET} (common) inputs may be used at any time without regard to the clock state. The flip-flop is set to the Q=1 state by applying a low level to the \overline{SET} input or reset to the Q=0 state by applying a low level to the \overline{RESET} input. If these inputs are not used they should be returned to a volt-

age between 2.0 and 5.5 Vdc.

Negative edge triggering — The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

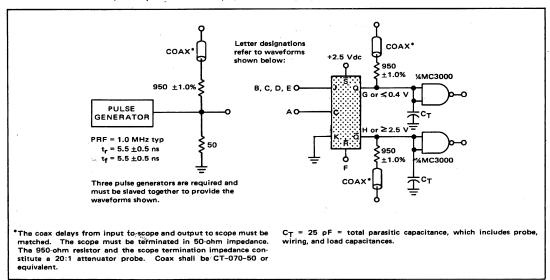
MAXIMUM CLOCK FREQUENCY TEST CIRCUIT VIHX = + 2.5 Vdc COAX* COAX 950 ±1.0% 14MC3000 950 ±1.0% +3.5 V -0 V -TPout TP_{in} $t_r = 5.5 \pm 0.5 \text{ ns}$ $t_f = 5.5 \pm 0.5 \text{ ns}$ ₹950 ₹±1.0% 14MC3000 Maximum Clock Frequency = 40 MHz min *The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent. C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

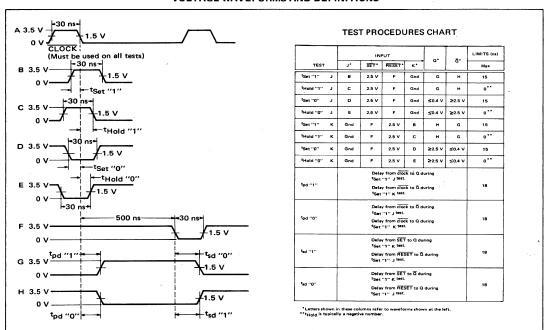


OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

(For J Inputs and RESET Input; to test other inputs, refer to Test Procedures Chart)





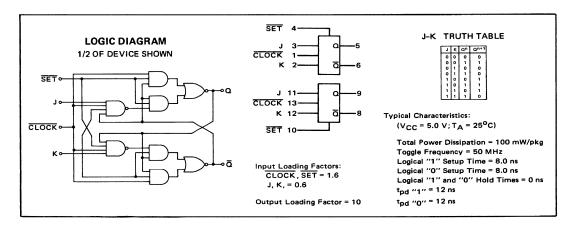
DUAL J-K FLIP-FLOP

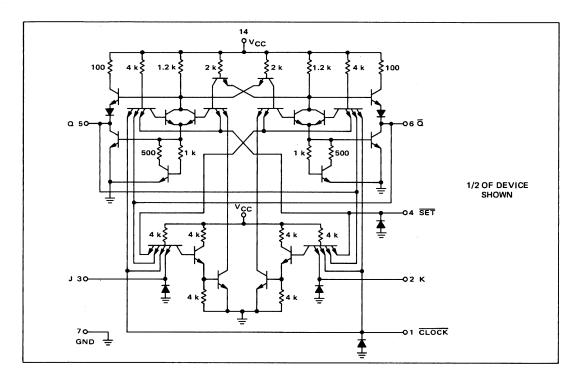
MC3062

The MC3062 dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct SET input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

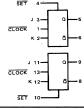
Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between

the Set-up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set-up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the SET input.





Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



1	TEST CURRENT/VOLTAGE VALUES														
@ Test		r	nA			Volts									
Temperature	lor	Іон	l _{in}	2l _{in}	l _D	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}			
0°C	23	-2.0	-	-	-	0.4	2.5	4.0	-	5.0	4.5	5.5			
+25°C	23	-2.0	1.0	2.0	-10	0.4	2.5	4.0	7.0	5.0	4.5	5.5			
+75°C	23	-2.0	-	-	-	0.4	2.5	4.0	-	5.0	4.5	5.5			

		Pin			3062 Test Limi		imits			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:													
Characteristic		Under	0°C		+25°C		+75°C			-			01		T 1/2	1,,	· V	v	T 1/2	·			0.1
	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	lor	ОН	lin	2I _{in}	l _D	٧ _F	V _R	V _{RH}	V _{max}	V _{cc}	VCCL	V _{CCH}	P ₁ *	Gnd
Input Forward Current	I _F	2	-	-1.5 -1.5	-	-1.5 -1.5	-	-1.5 -1.5	mAdc mAdc	- -	-	-	- -	-	2 3	- -	1,4 1,4	-	-	<u>-</u>	14 14	- -	3,6,7,13 2,5,7,13
	I _{FS}	4	-	-1.8	-	-1.8	-	-1.8	mAdc	-	-	-	-	-	4	-	1,2	-	-	-	14	-	3,7,13
	^I FĈ	1	-	-2.9 -2.9	-	-2. 9 -2. 9	-	-2.9 -2.9	m Adc m Adc	-	-	-	-	-	1 1	-	2,3 2,3,4	-	-	-	14 14	4 5	7,13 7,13
Leakage Current	I _R	2 3	-	80 80	-	80 80	-	80 80	μAdc μAdc	-	-	-	-	-	-	2 3	3 2	· -	-		14 14	-	1,4,7,13 1,4,7,13
	I _{RS}	4	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	4	3	-	-	-	14	-	1,2,7,13
ų.	I _R C	1		170	-	170	-	170	μAdc	-	-	-	-	- ,	-	1	-	-	-	-	14	-	2,3,4,7,13
Breakdown Voltage	BV _{in}	2 3 4 1			5.5	1 2 1 -		-	Vdc	- - -	1111	2 3 - -	- 4 1	-				- - -	1.1	1111	14		1,4,7,13 1,4,7,13 1,2,7,13 2,3,4,7,13
Clamp Voltage	v _D	2 3 4 1	-			-1.5	-	-	Vdc	-	1111		-	2 3 4 1		- - -	- - -	- - -	-	14	-		7,13
Output																				-			
Output Voltage	VOL	5 6	- -	0.4 0.4	-	0.4 0.4	- -	0.4 0.4	Vdc Vdc	5 6		-	-	-	4	-	-	-	-	-	14 14	5 4	1,7,13 1,7,13
	Vон	5 6	2. 5 2. 5	- 1 - 1	2.5 2.5	-	2.5 2.5	-	Vdc Vdc	-	5 6	-	-	- 1	4	-	4	-	- 1	14 14	- 1 	4 5	7 1,7,13
Short-Circuit Current	I _{SC}	5	-	-	-20	-60	-	-	mAdc	-	-	-	- 1	-	-	-	-	-	14	-	-	-	4,5,7,13
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	41	-	-	mAdc	-	-	-	-	-	11	-	-	14	-	-	-	-	4,7,10
Power Supply Drain	I_{PD}	14	-	29	-	29	-	29	mAdc	-	-	-	-	-	-	-	-	- :	14	-	-	-	4,7,10

^{*} Momentarily ground pin prior to taking measurement. (If pin is also in another column the pin must be returned to that voltage or current for measurement.)

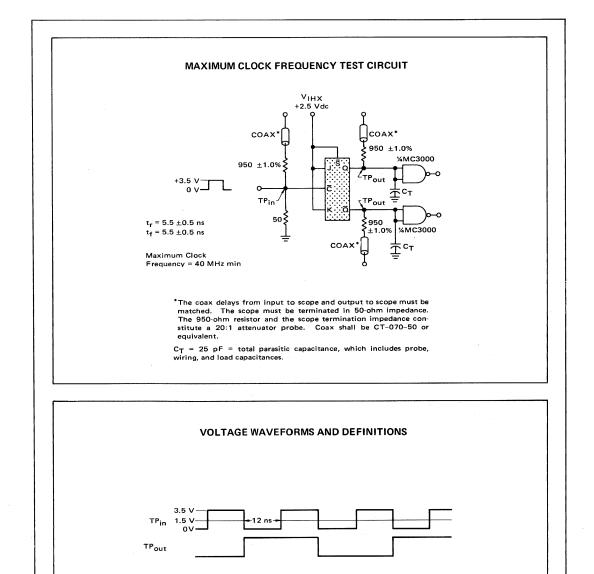
OPERATING CHARACTERISTICS

The data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The flip-flop is set to the Ω = 1 state by applying a low level to the SET input. The direct SET inputs may be used at any time without regard to the clock state. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering — The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.



OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

(For J Inputs; to test other inputs, refer to Test Procedures Chart)

